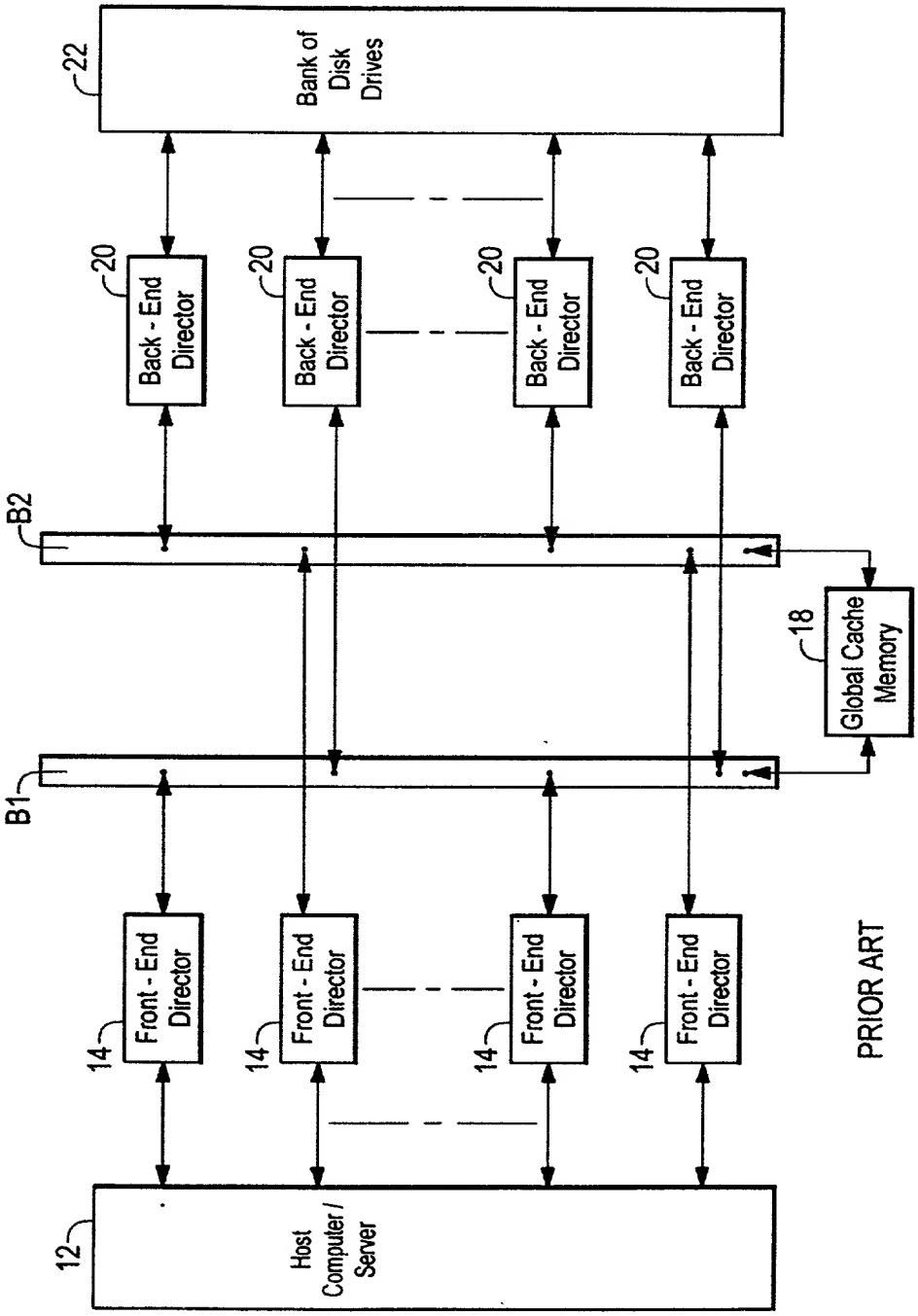


PRIOR ART

FIG. 1

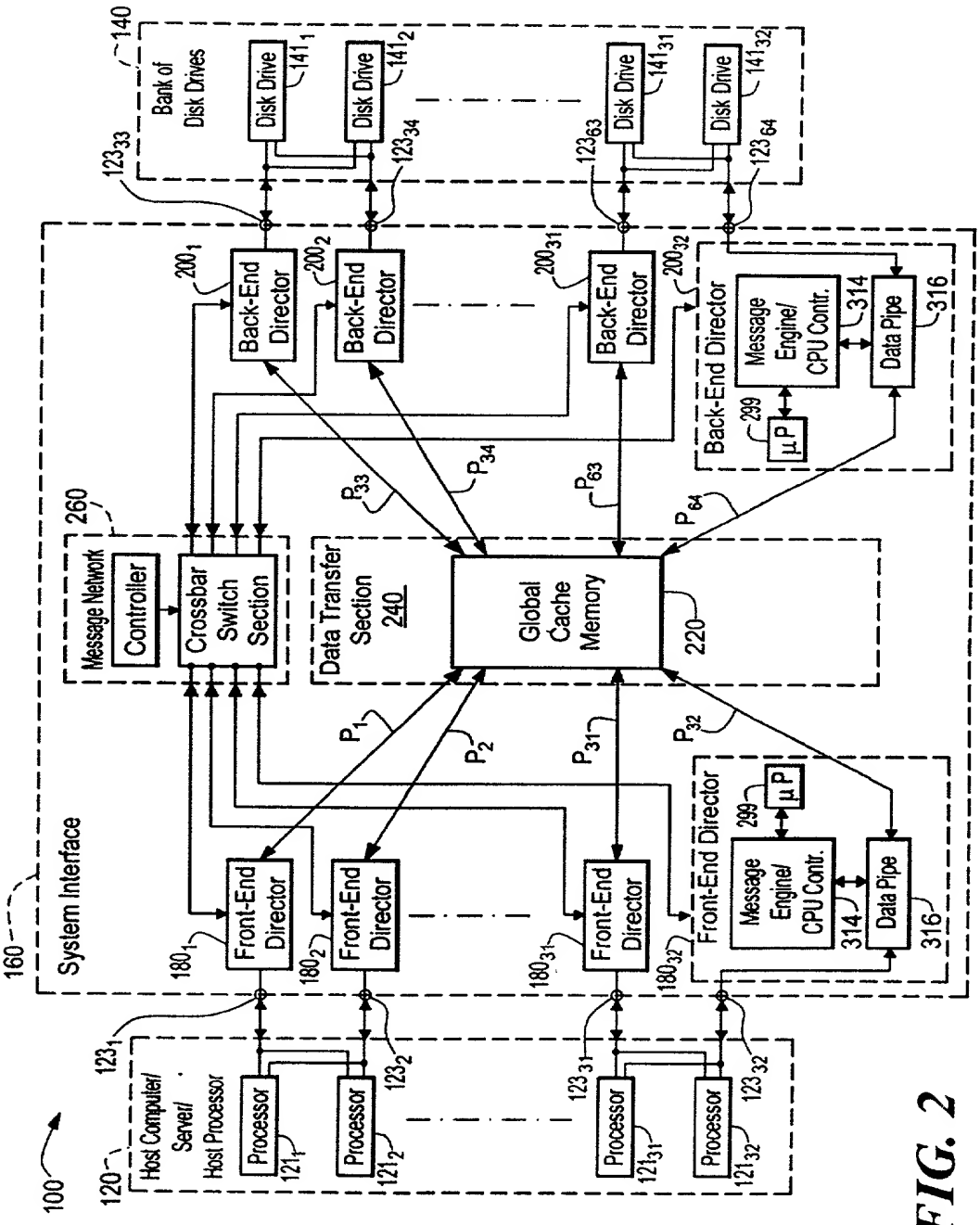

100
120
Host Computer/ Server/ Host Processor
Processor
121_1
121_2
121_{31}
121_{32}
123_1
123_2
123_{31}
123_{32}
160
System Interface
180_1
180_2
180_{31}
180_{32}
Front-End Director
Front-End Director
Front-End Director
Front-End Director
μP
299
Message Engine/ CPU Contr.
314
Data Pipe
316
260
Message Network
Controller
Crossbar Switch Section
Data Transfer Section 240
Global Cache Memory
220
P_1
P_2
P_{31}
P_{32}
P_{33}
P_{34}
P_{63}
P_{64}
200_1
200_2
200_{31}
200_{32}
Back-End Director
Back-End Director
Back-End Director
Back-End Director
Message Engine/ CPU Contr.
314
Data Pipe
316
μP
299
140
Bank of Disk Drives
Disk Drive
141_1
141_2
141_{31}
141_{32}
123_{33}
123_{34}
123_{63}
123_{64}

FIG. 2

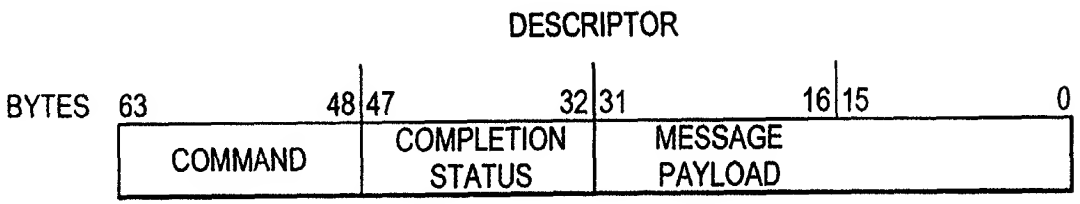


FIG. 2A

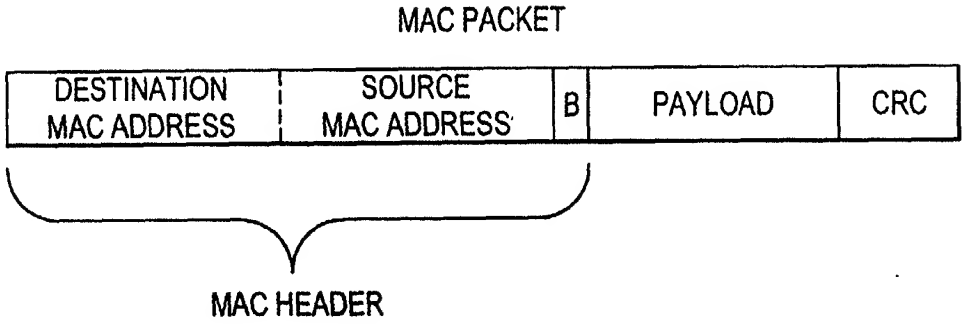


FIG. 2B

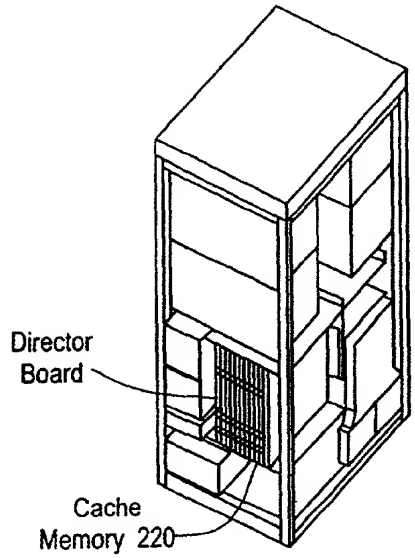


FIG. 3

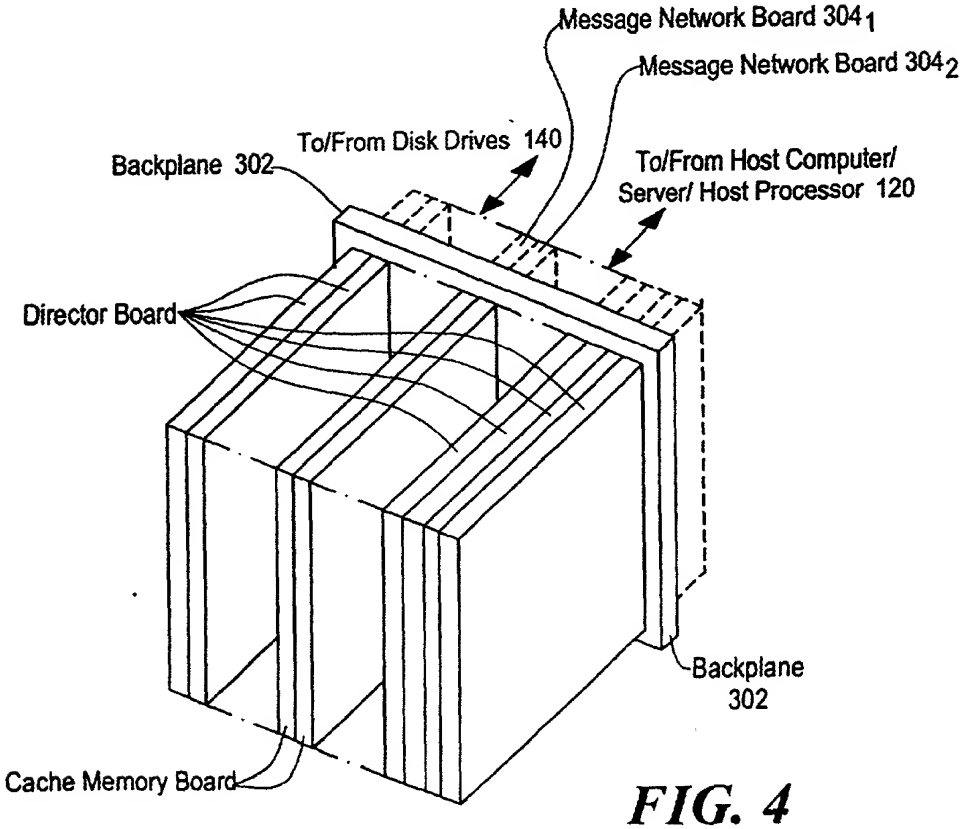
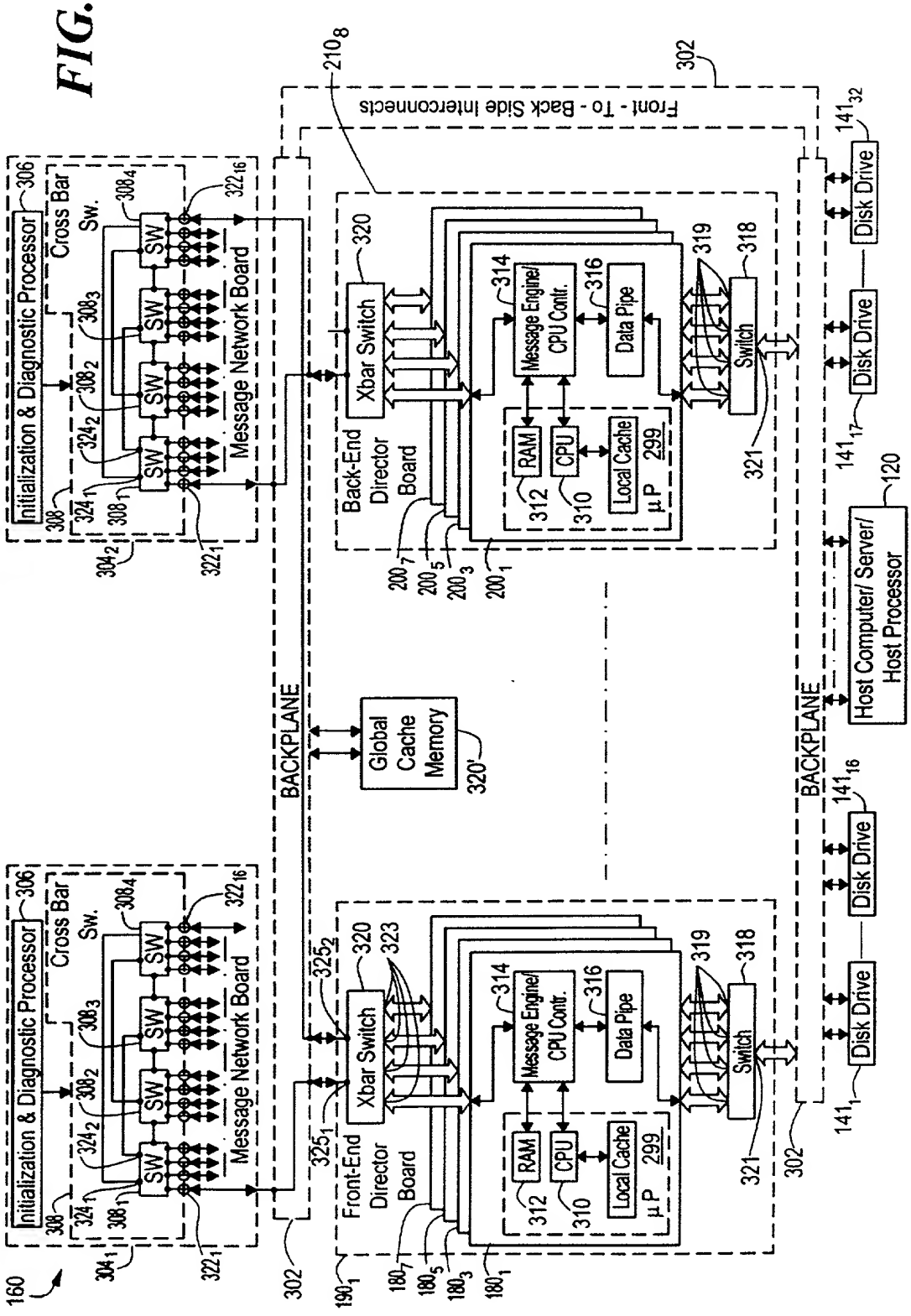


FIG. 4

FIG. 5


160
Initialization & Diagnostic Processor
306
Cross Bar Sw.
Message Network Board
SW
308
BACKPLANE
302
Front-End Director Board
Back-End Director Board
Xbar Switch
320
323
Global Cache Memory
320'
Message Engine/ CPU Contr.
314
Data Pipe
316
RAM
312
CPU
310
Local Cache µP
299
Switch
318
319
321
Front - To - Back Side Interconnects
Host Computer/ Server/ Host Processor
120
Disk Drive

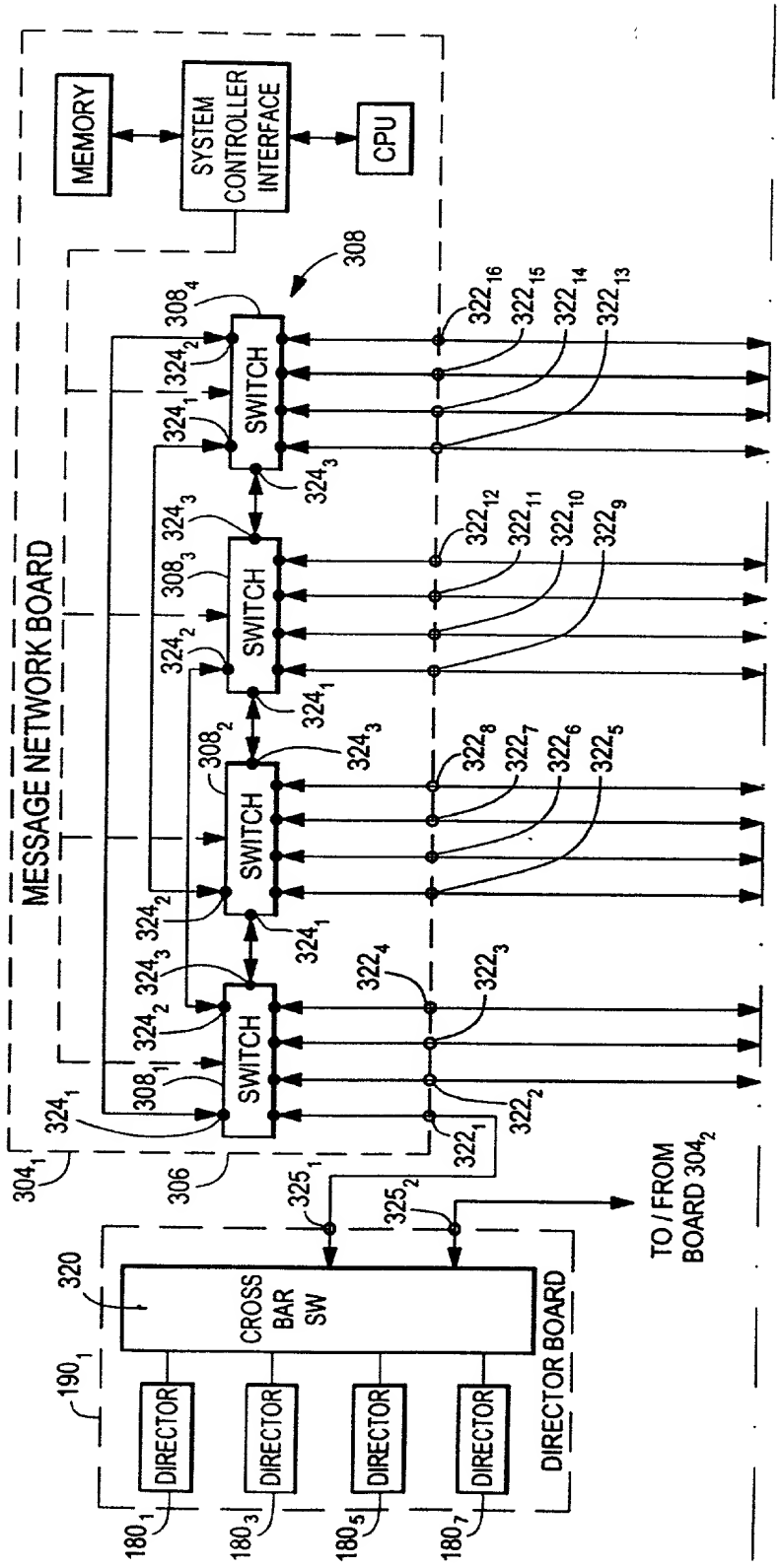


FIG. 6A

FIG. 6

FIG. 6A
FIG. 6B

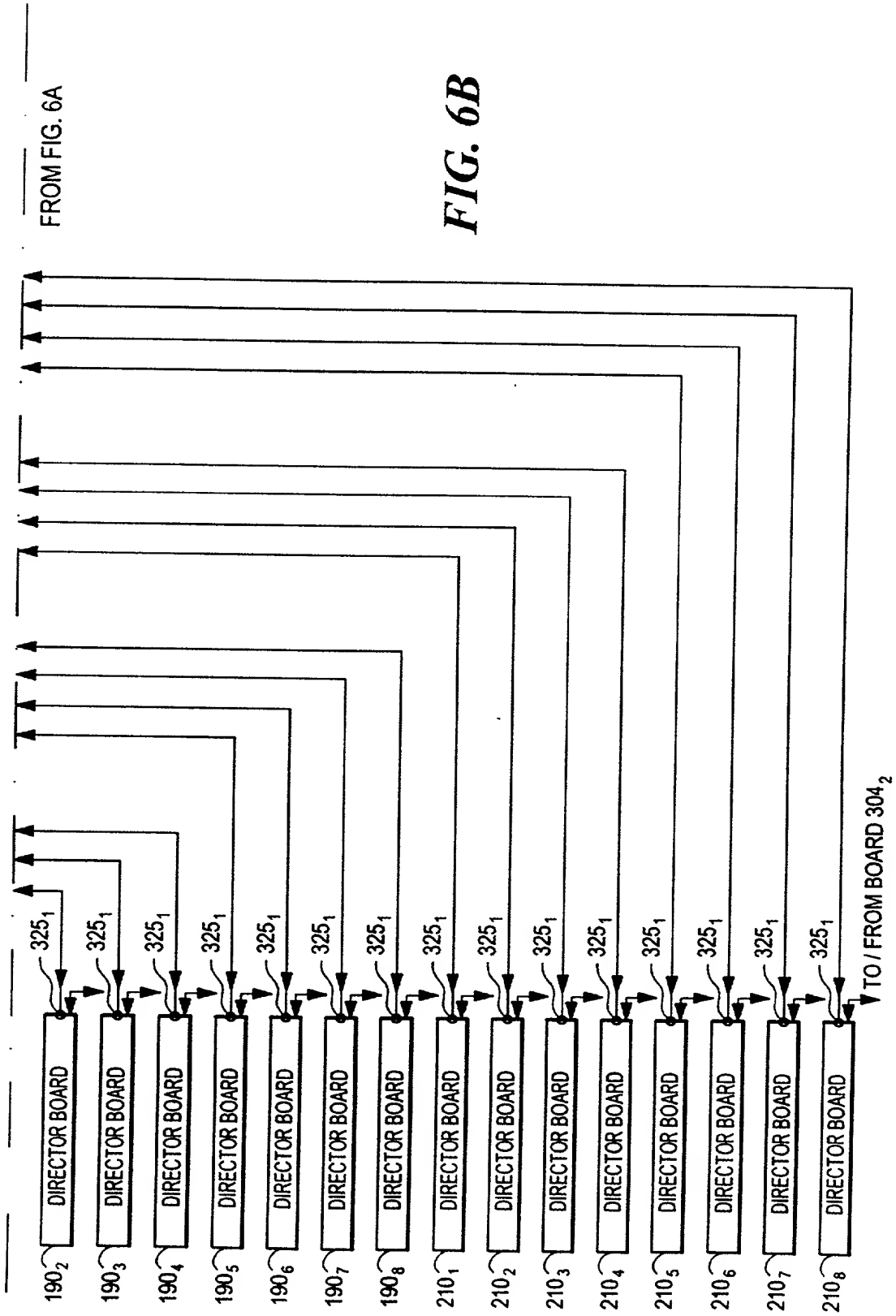

FROM FIG. 6A
DIRECTOR BOARD
190_2
190_3
190_4
190_5
190_6
190_7
190_8
210_1
210_2
210_3
210_4
210_5
210_6
210_7
210_8
325_1
TO / FROM BOARD 304_2

FIG. 6B

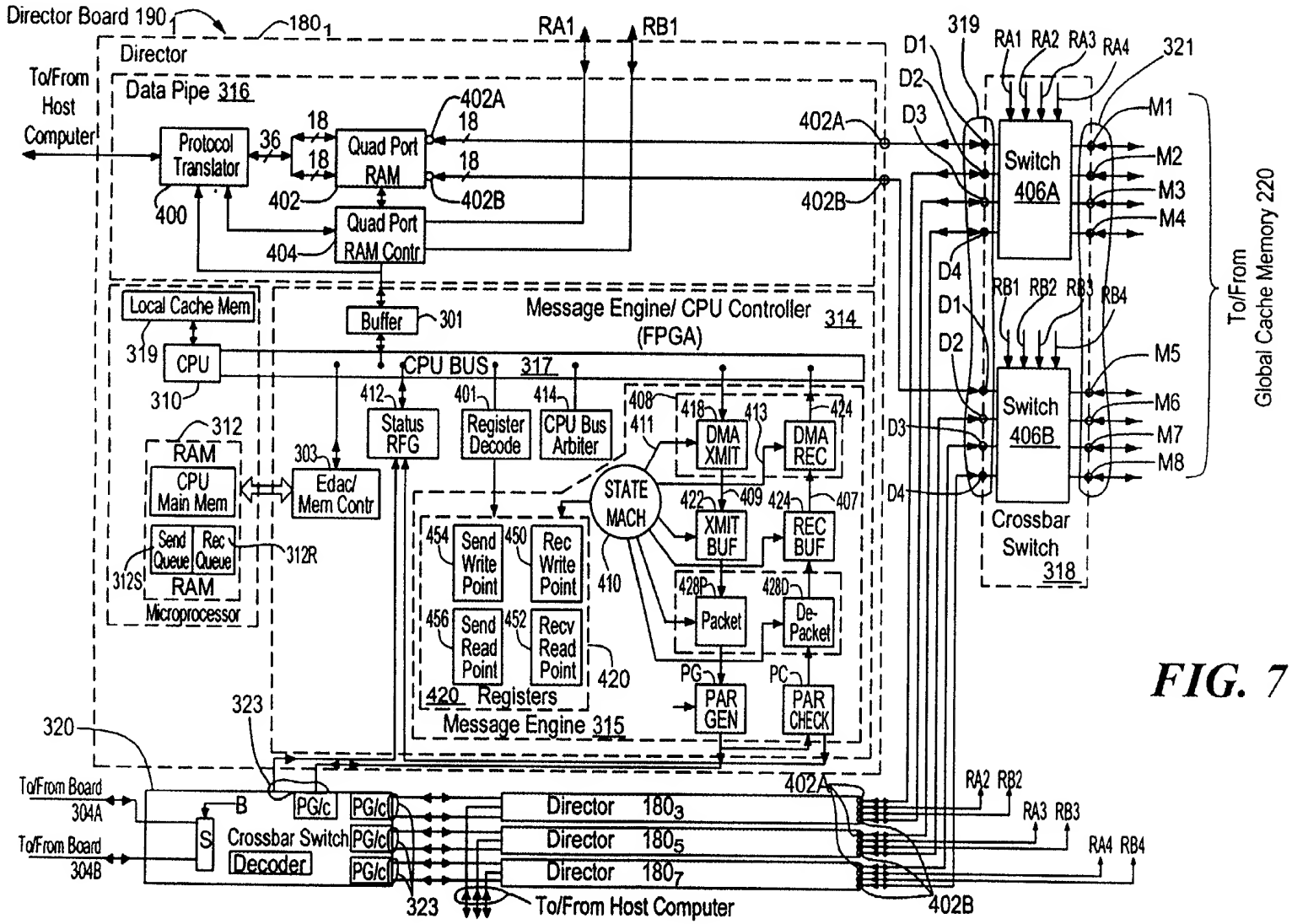


FIG. 7

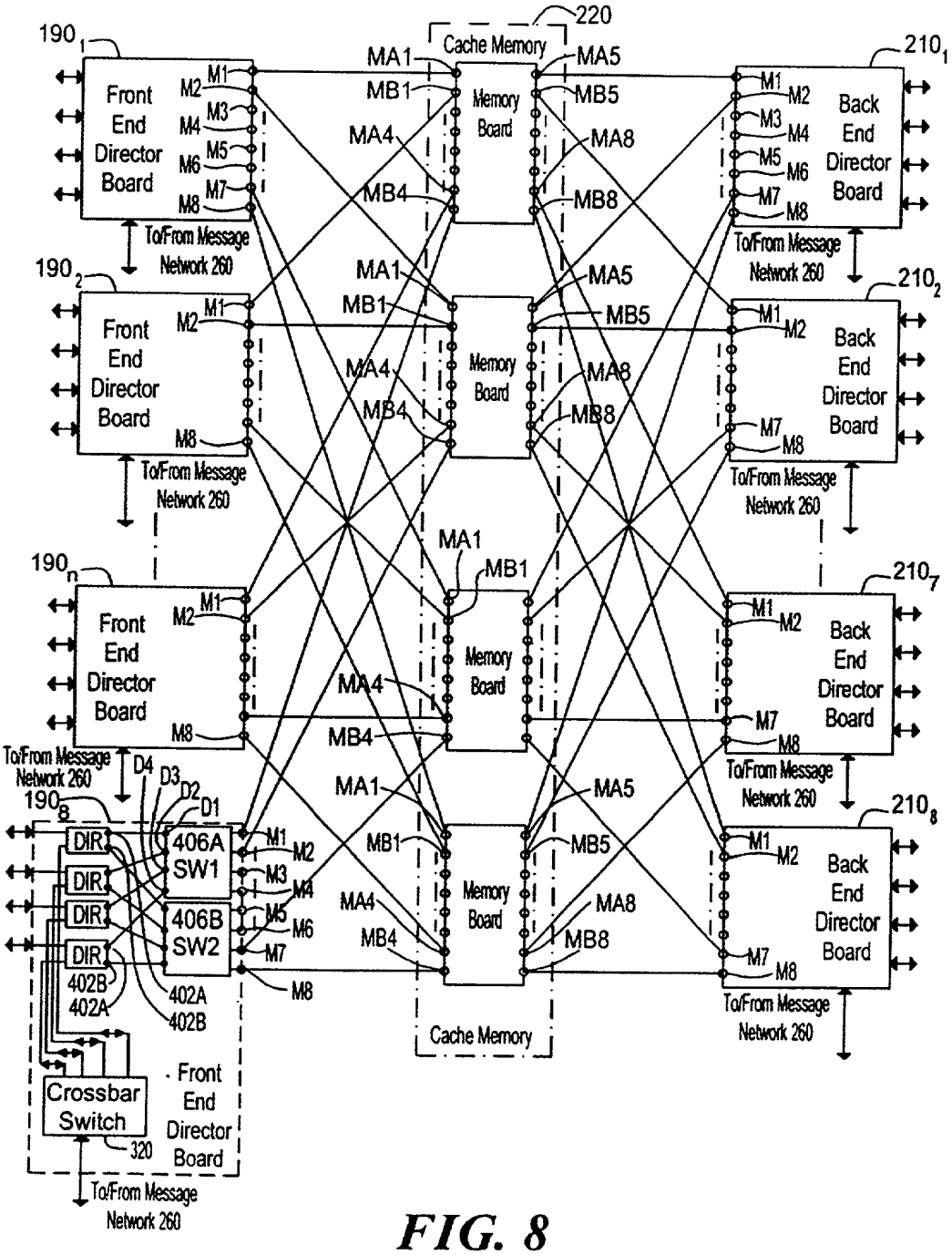

190 1
190 2
190 n
190 8
Front End Director Board
To/From Message Network 260
220
Cache Memory
Memory Board
210 1
210 2
210 7
210 8
Back End Director Board
M1
M2
M3
M4
M5
M6
M7
M8
MA1
MB1
MA4
MB4
MA5
MB5
MA8
MB8
D1
D2
D3
D4
DIR
406A SW1
406B SW2
402A
402B
Crossbar Switch
320

FIG. 8

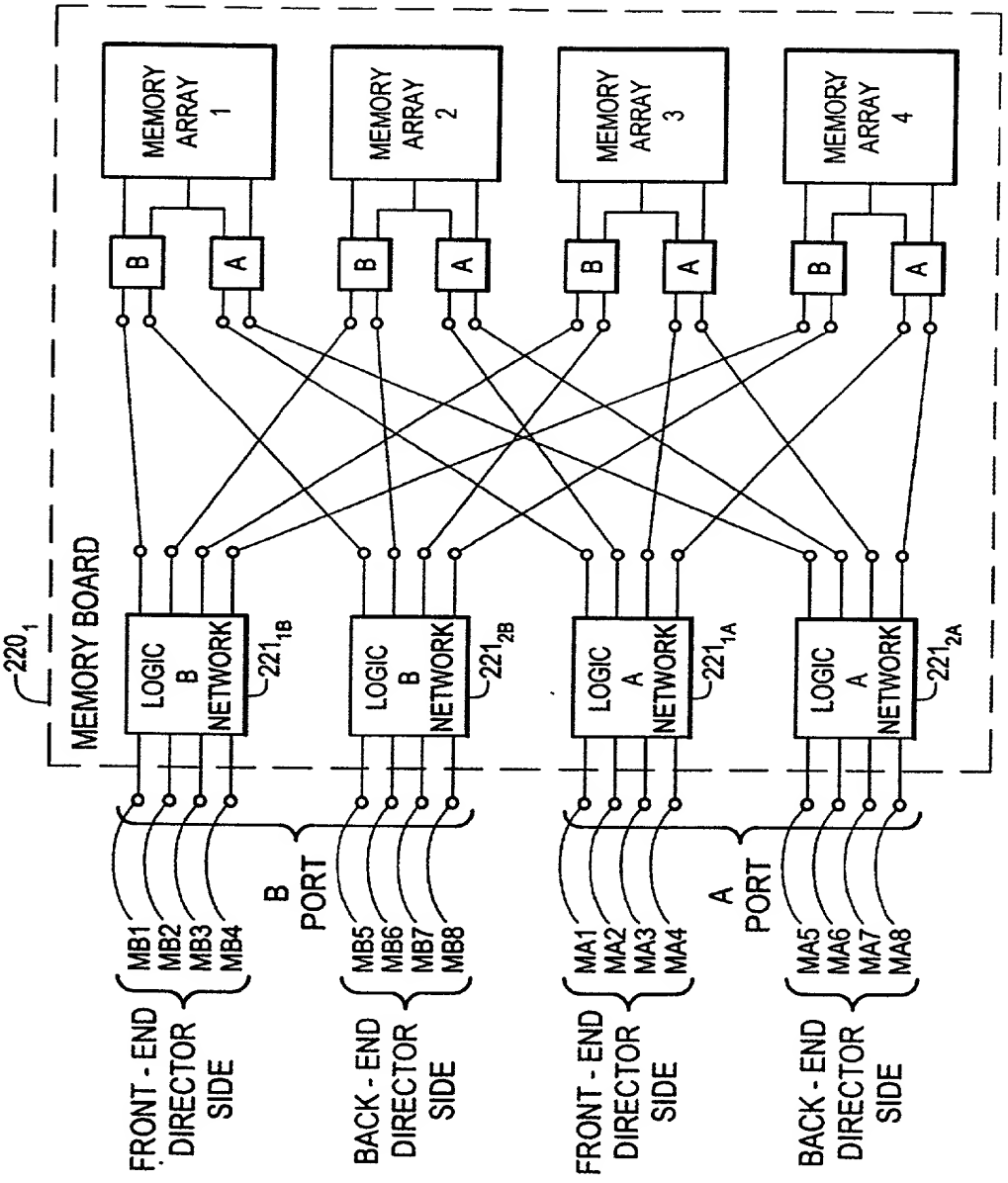

MEMORY BOARD
220₁
LOGIC B NETWORK
221₁B
LOGIC B NETWORK
221₂B
LOGIC A NETWORK
221₁A
LOGIC A NETWORK
221₂A
MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4
B
A
B PORT
A PORT
MB1
MB2
MB3
MB4
MB5
MB6
MB7
MB8
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
FRONT - END DIRECTOR SIDE
BACK - END DIRECTOR SIDE
FRONT - END DIRECTOR SIDE
BACK - END DIRECTOR SIDE

FIG. 8A

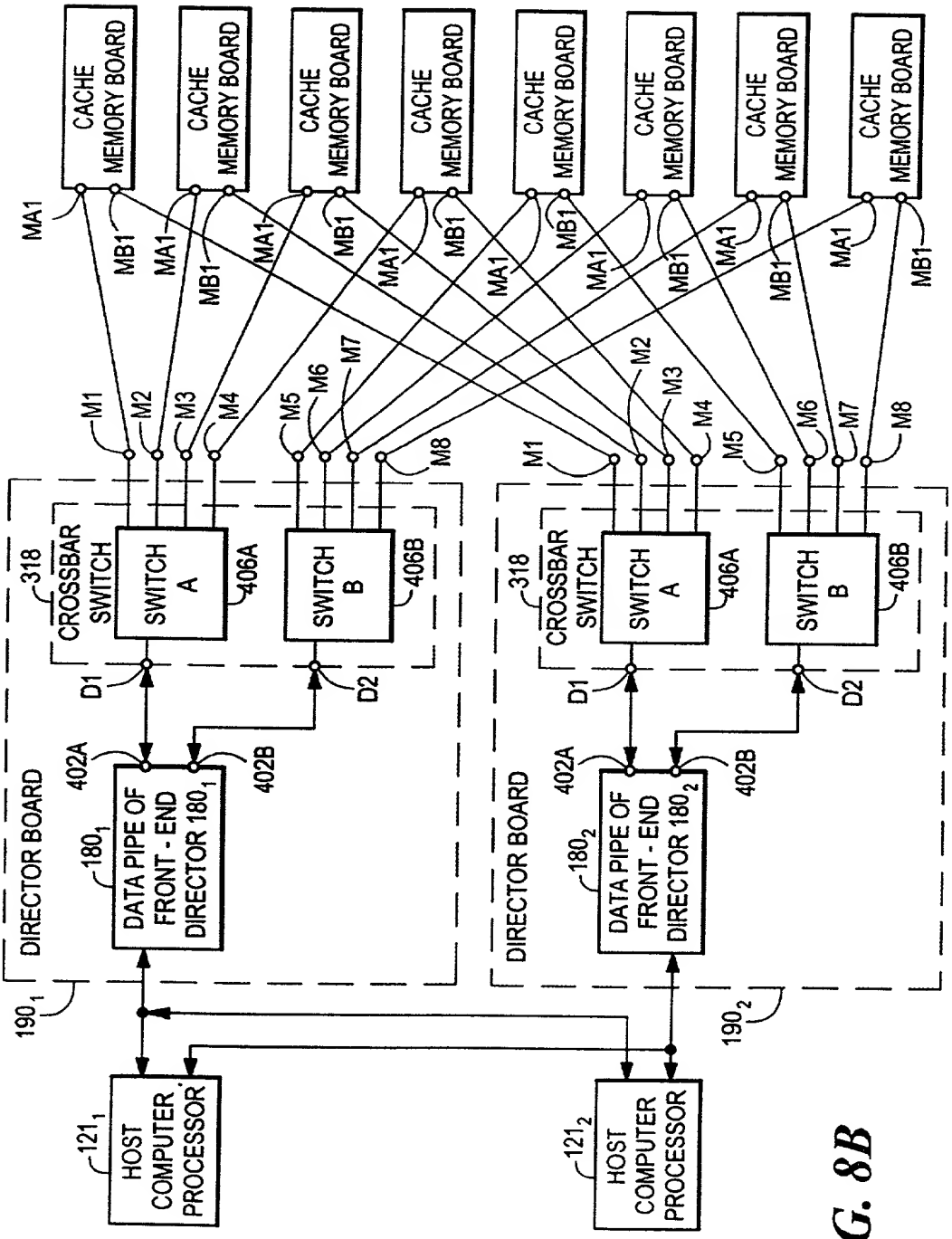

CACHE MEMORY BOARD
MA1
MB1
M1
M2
M3
M4
M5
M6
M7
M8
318
CROSSBAR SWITCH
SWITCH A
406A
SWITCH B
406B
D1
D2
402A
402B
DIRECTOR BOARD
190_1
190_2
180_1
180_2
DATA PIPE OF FRONT - END DIRECTOR 180_1
DATA PIPE OF FRONT - END DIRECTOR 180_2
121_1
121_2
HOST COMPUTER PROCESSOR

FIG. 8B

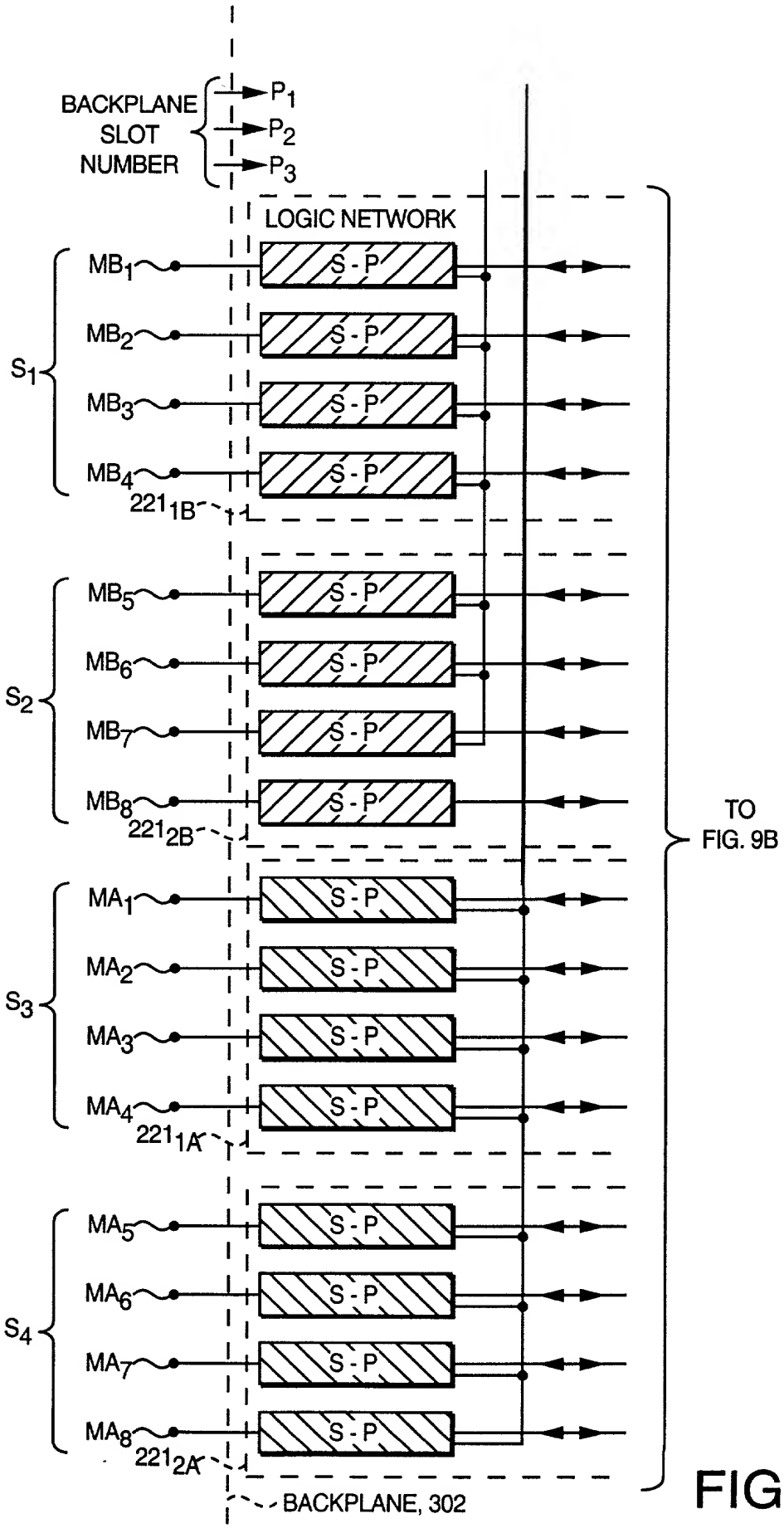
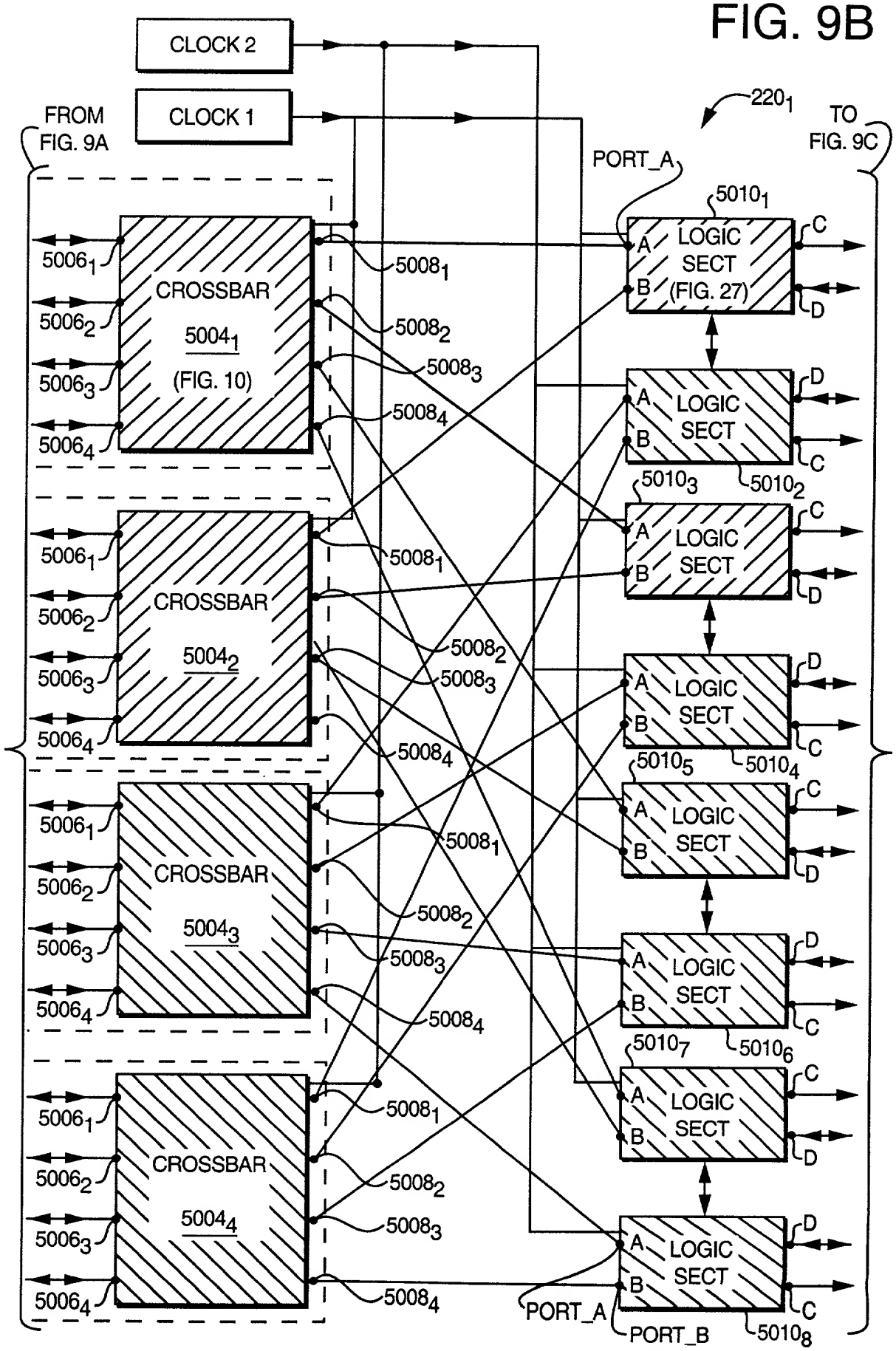

BACKPLANE SLOT NUMBER
P1
P2
P3
LOGIC NETWORK
MB1
MB2
MB3
MB4
S1
221 1B
MB5
MB6
MB7
MB8
S2
221 2B
TO FIG. 9B
MA1
MA2
MA3
MA4
S3
221 1A
MA5
MA6
MA7
MA8
S4
221 2A
S - P
BACKPLANE, 302

FIG. 9A

FIG. 9B


CLOCK 2
CLOCK 1
FROM FIG. 9A
TO FIG. 9C
220_1
PORT_A
5010_1
5006_1
5006_2
5006_3
5006_4
CROSSBAR 5004_1 (FIG. 10)
5008_1
5008_2
5008_3
5008_4
CROSSBAR 5004_2
CROSSBAR 5004_3
CROSSBAR 5004_4
LOGIC SECT (FIG. 27)
LOGIC SECT
A
B
C
D
5010_2
5010_3
5010_4
5010_5
5010_6
5010_7
5010_8
PORT_A
PORT_B

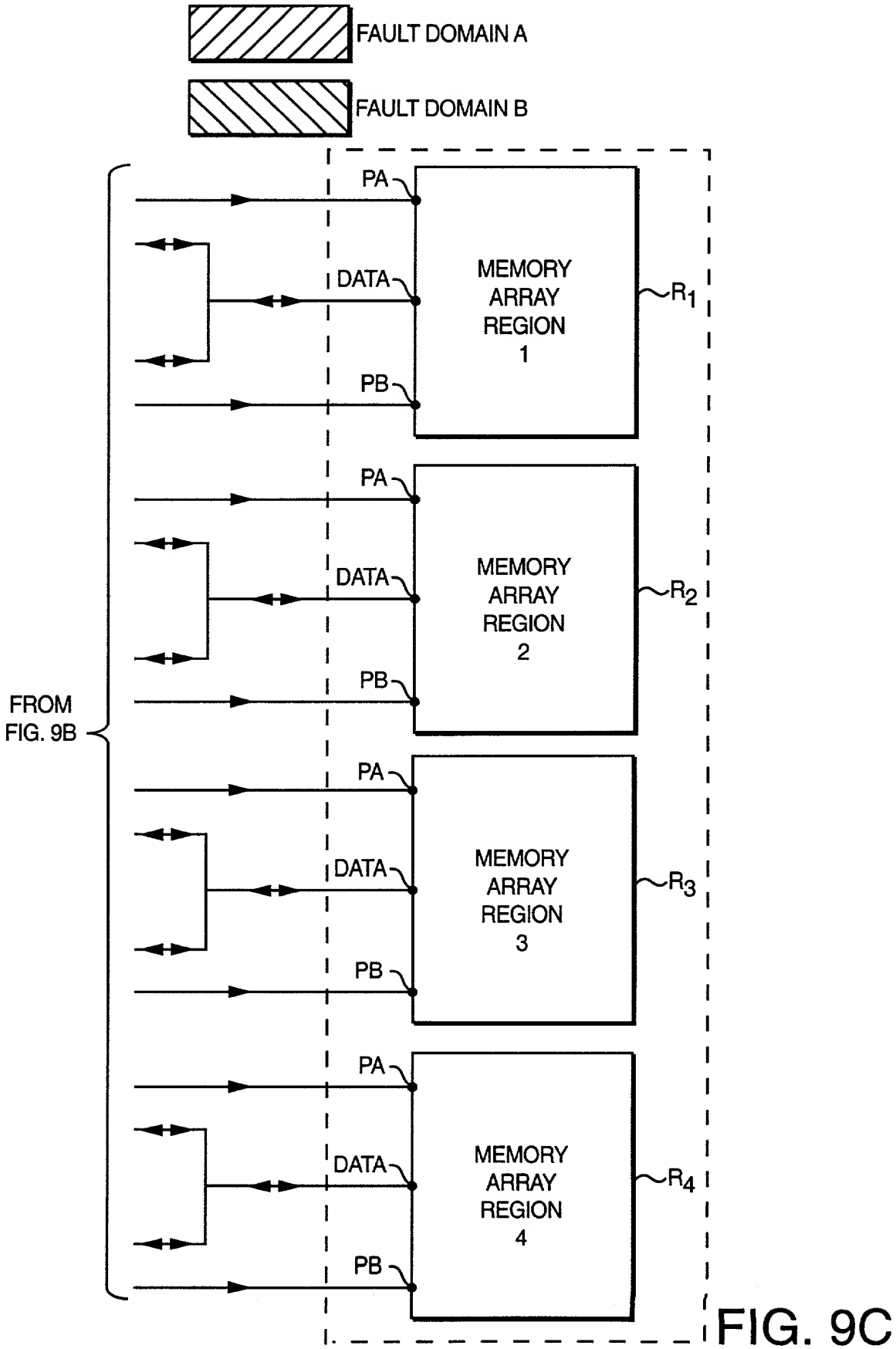
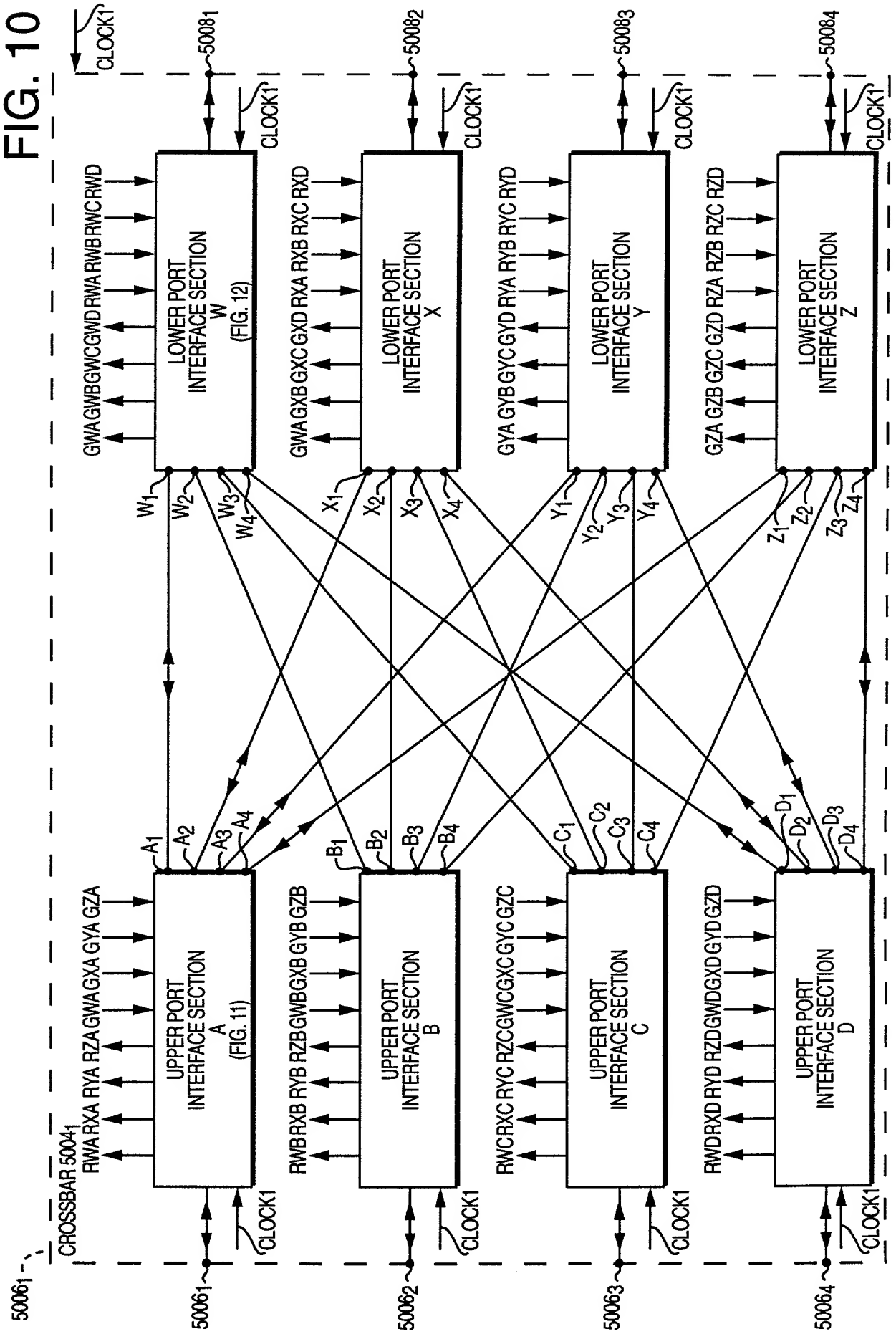

FAULT DOMAIN A
FAULT DOMAIN B
FROM FIG. 9B
PA
DATA
PB
MEMORY ARRAY REGION 1
R1
MEMORY ARRAY REGION 2
R2
MEMORY ARRAY REGION 3
R3
MEMORY ARRAY REGION 4
R4

FIG. 9C

FIG. 10


CROSSBAR 50041
50061
50062
50063
50064
CLOCK1
RWA RXA RYA RZA GWA GXA GYA GZA
RWB RXB RYB RZB GWB GXB GYB GZB
RWC RXC RYC RZC GWC GXC GYC GZC
RWD RXD RYD RZD GWD GXD GYD GZD
UPPER PORT INTERFACE SECTION A (FIG. 11)
UPPER PORT INTERFACE SECTION B
UPPER PORT INTERFACE SECTION C
UPPER PORT INTERFACE SECTION D
A1 A2 A3 A4
B1 B2 B3 B4
C1 C2 C3 C4
D1 D2 D3 D4
GWA GWB GWC GWD RWA RWB RWC RWD
GXA GXB GXC GXD RXA RXB RXC RXD
GYA GYB GYC GYD RYA RYB RYC RYD
GZA GZB GZC GZD RZA RZB RZC RZD
LOWER PORT INTERFACE SECTION W (FIG. 12)
LOWER PORT INTERFACE SECTION X
LOWER PORT INTERFACE SECTION Y
LOWER PORT INTERFACE SECTION Z
W1 W2 W3 W4
X1 X2 X3 X4
Y1 Y2 Y3 Y4
Z1 Z2 Z3 Z4
50081
50082
50083
50084

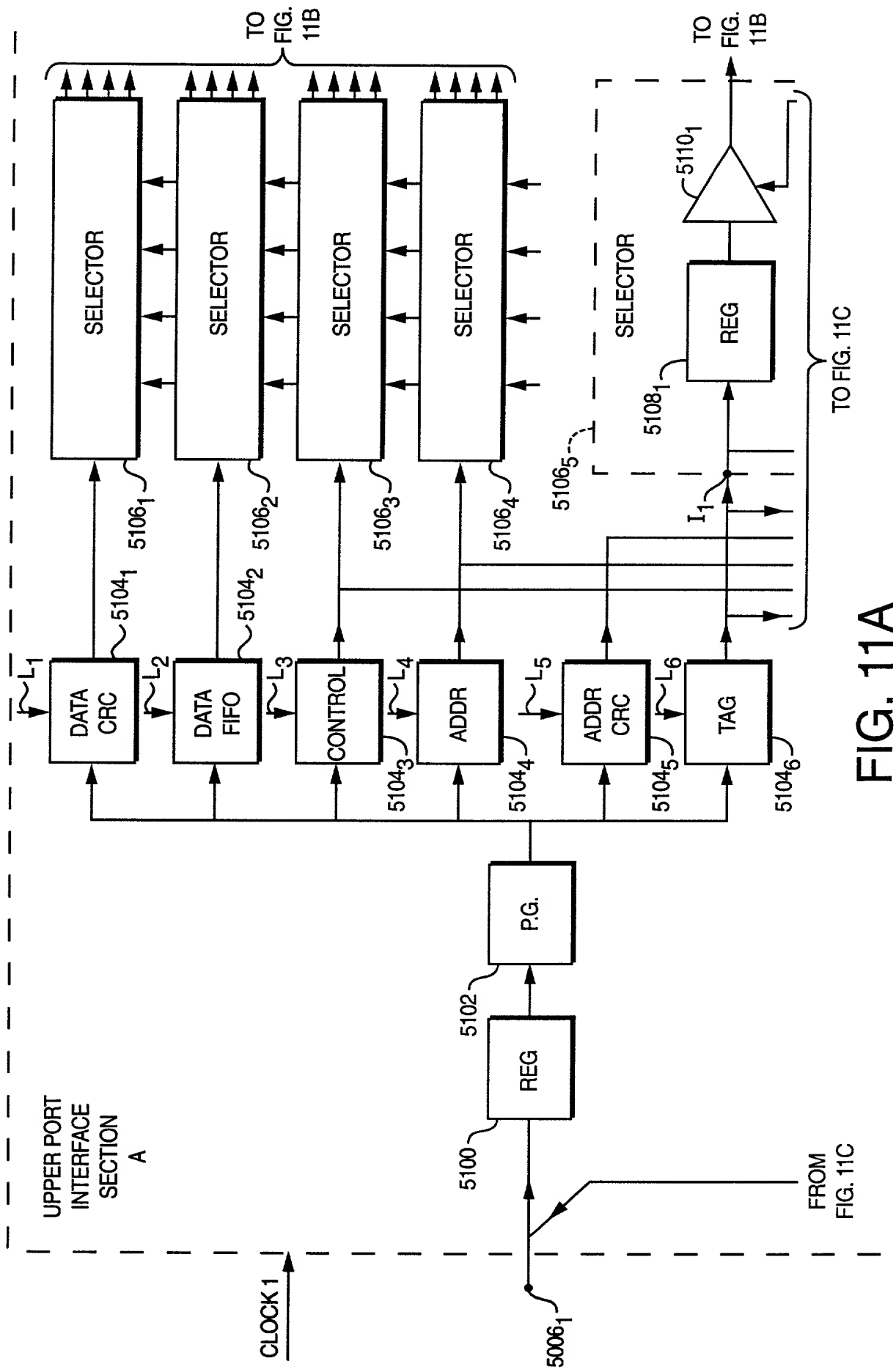
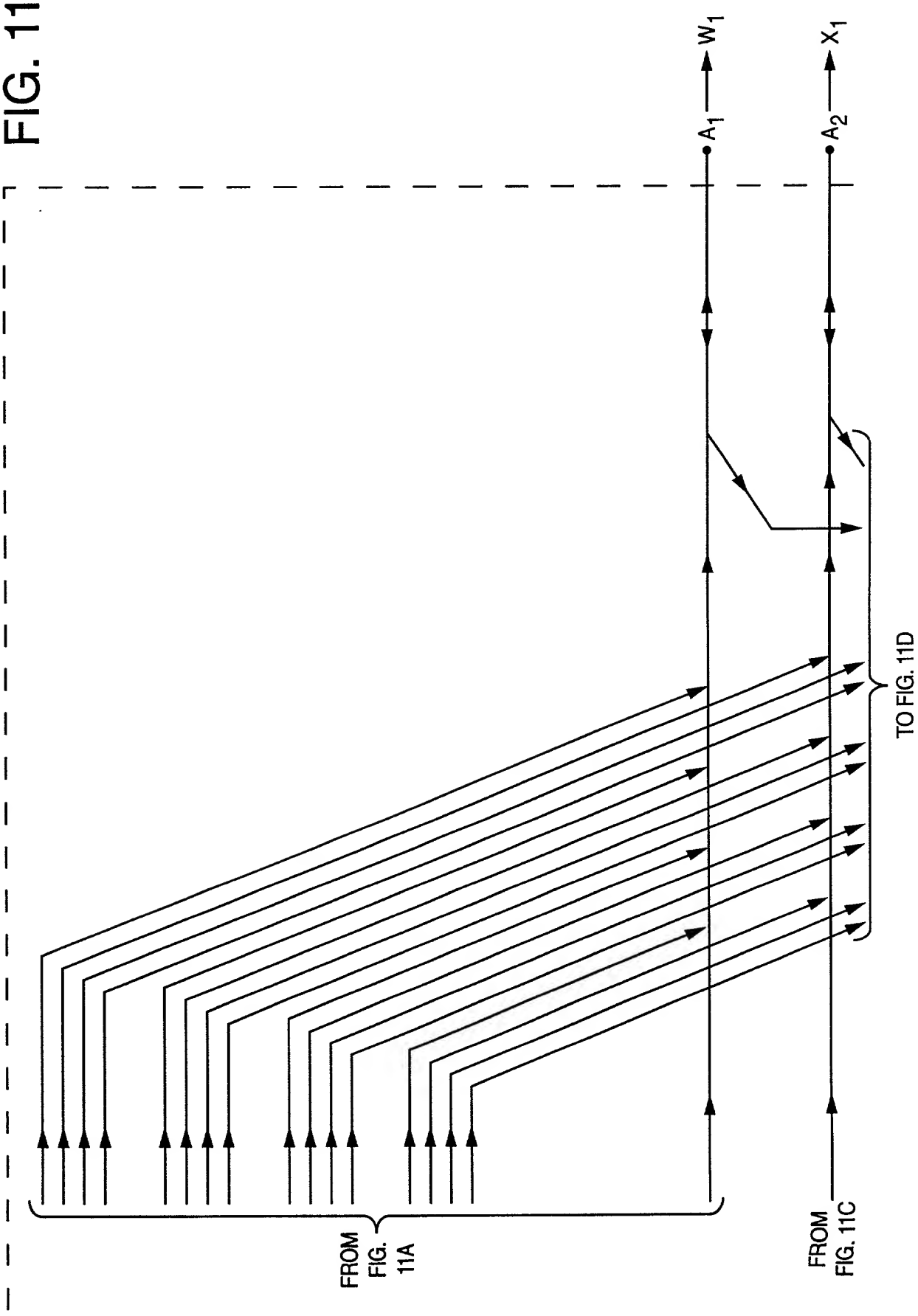

TO FIG. 11B
TO FIG. 11B
SELECTOR
SELECTOR
SELECTOR
SELECTOR
SELECTOR
REG
TO FIG. 11C
DATA CRC
DATA FIFO
CONTROL
ADDR
ADDR CRC
TAG
P.G.
REG
UPPER PORT INTERFACE SECTION A
FROM FIG. 11C
CLOCK 1
5100
5102
5006₁
5104₁
5104₂
5104₃
5104₄
5104₅
5104₆
5106₁
5106₂
5106₃
5106₄
5106₅
5108₁
5110₁
I₁
L₁
L₂
L₃
L₄
L₅
L₆

FIG. 11A

FIG. 11B



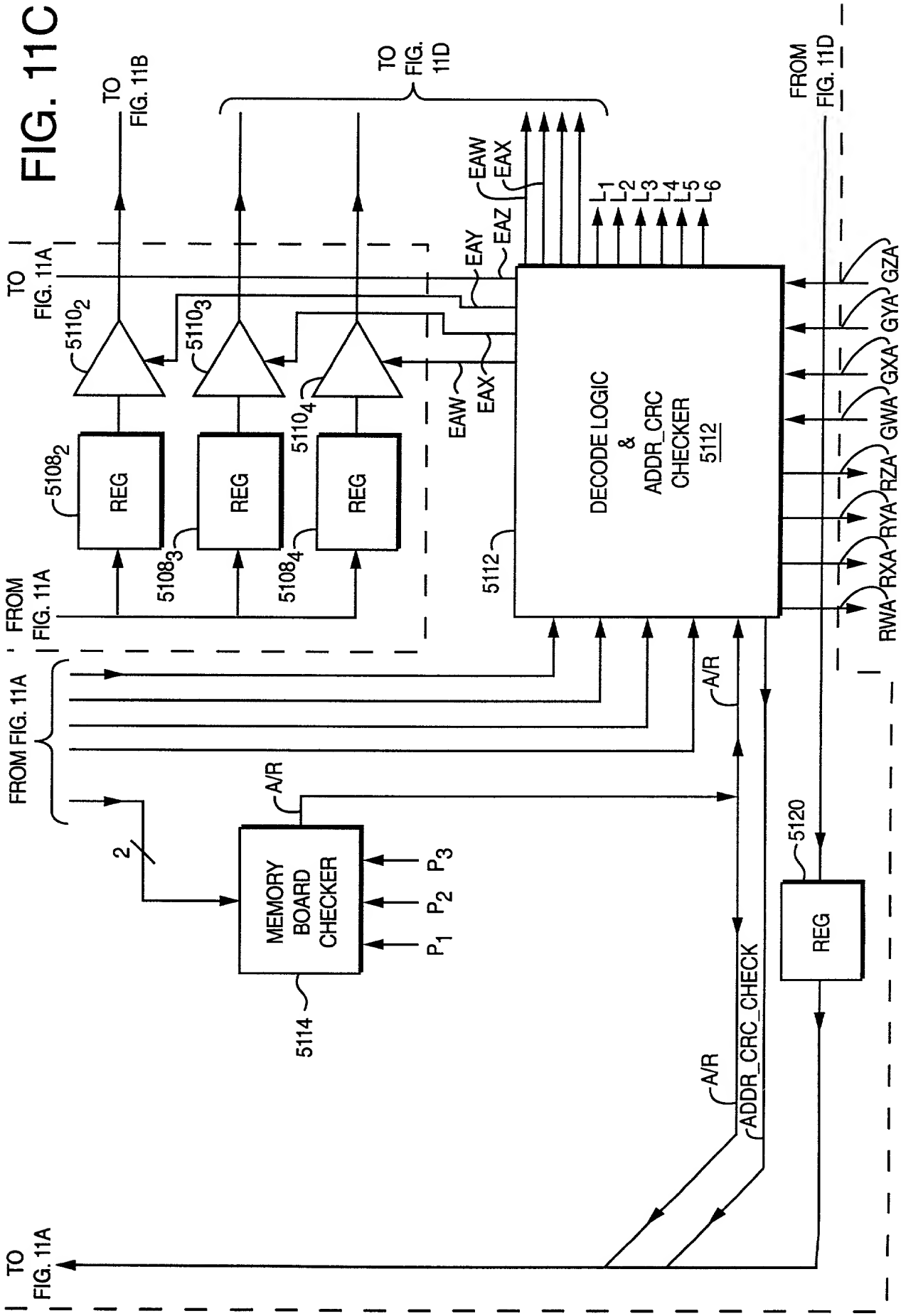

TO FIG. 11B
TO FIG. 11D
FROM FIG. 11D
TO FIG. 11A
FROM FIG. 11A
FROM FIG. 11A
TO FIG. 11A
5110₂
5110₃
5110₄
5108₂
5108₃
5108₄
REG
REG
REG
EAW
EAX
EAY
EAZ
L1
L2
L3
L4
L5
L6
DECODE LOGIC & ADDR_CRC CHECKER 5112
5112
GZA
GYA
GXA
GWA
RZA
RYA
RXA
RWA
A/R
2
MEMORY BOARD CHECKER
P1 P2 P3
5114
A/R
ADDR_CRC_CHECK
5120
REG

FIG. 11C

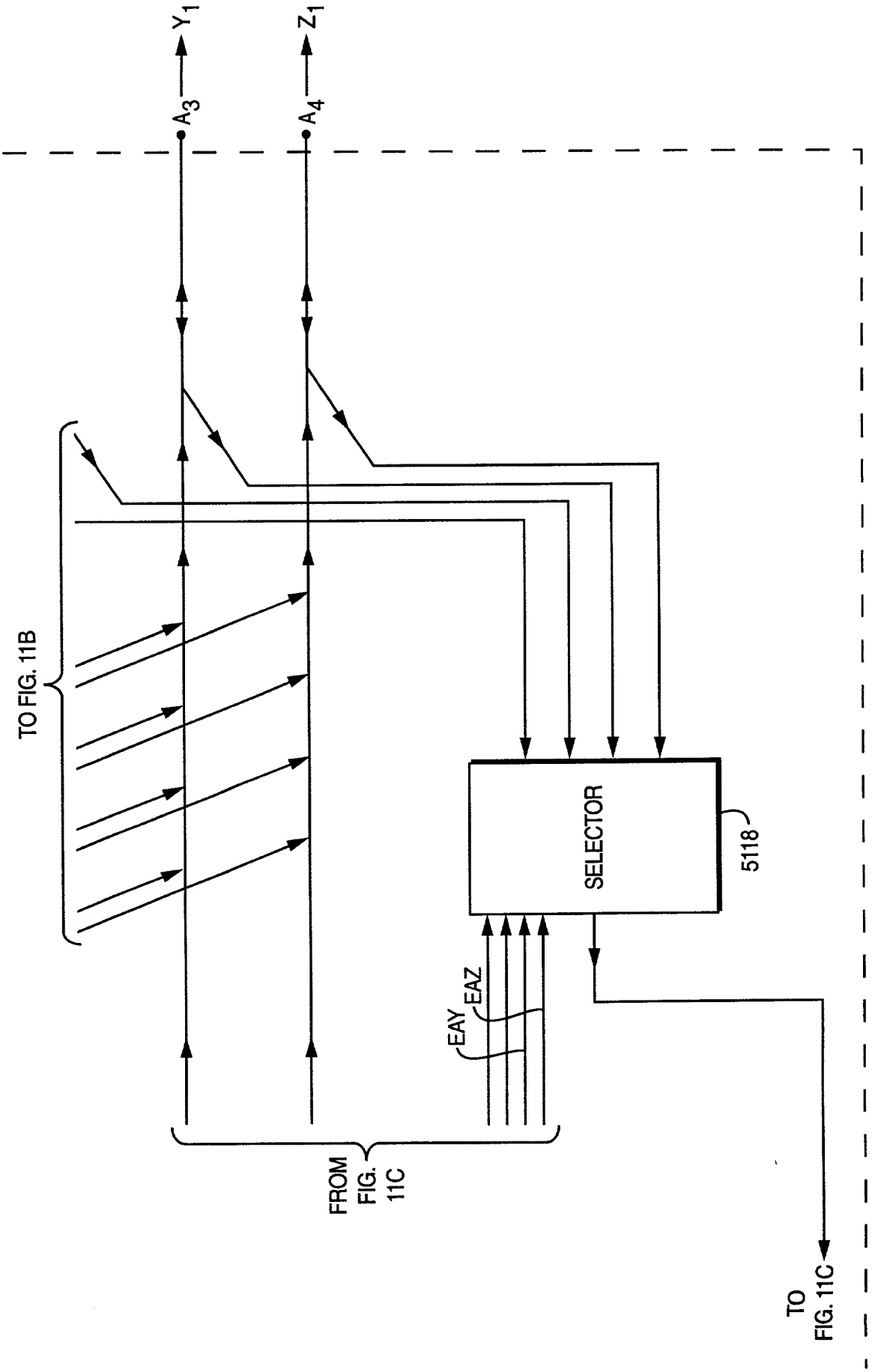

Y_1
Z_1
A_3
A_4
TO FIG. 11B
SELECTOR
5118
EAY
EAZ
FROM FIG. 11C
TO FIG. 11C

FIG. 11D

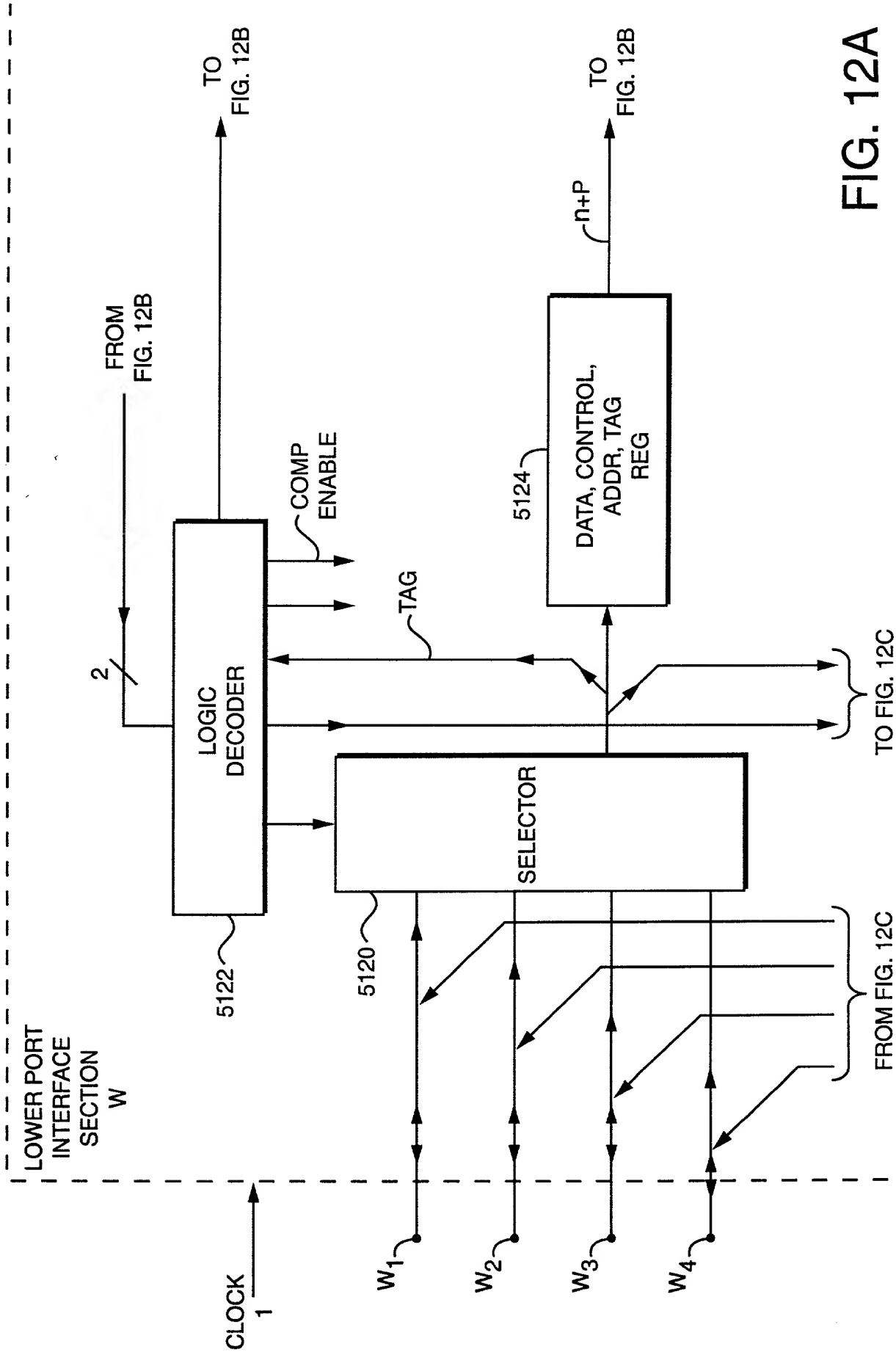

LOWER PORT INTERFACE SECTION W
CLOCK
1
FROM FIG. 12B
2
LOGIC DECODER
5122
COMP ENABLE
TAG
TO FIG. 12B
5120
SELECTOR
5124
DATA, CONTROL, ADDR, TAG REG
n+P
TO FIG. 12B
TO FIG. 12C
FROM FIG. 12C
W1
W2
W3
W4

FIG. 12A

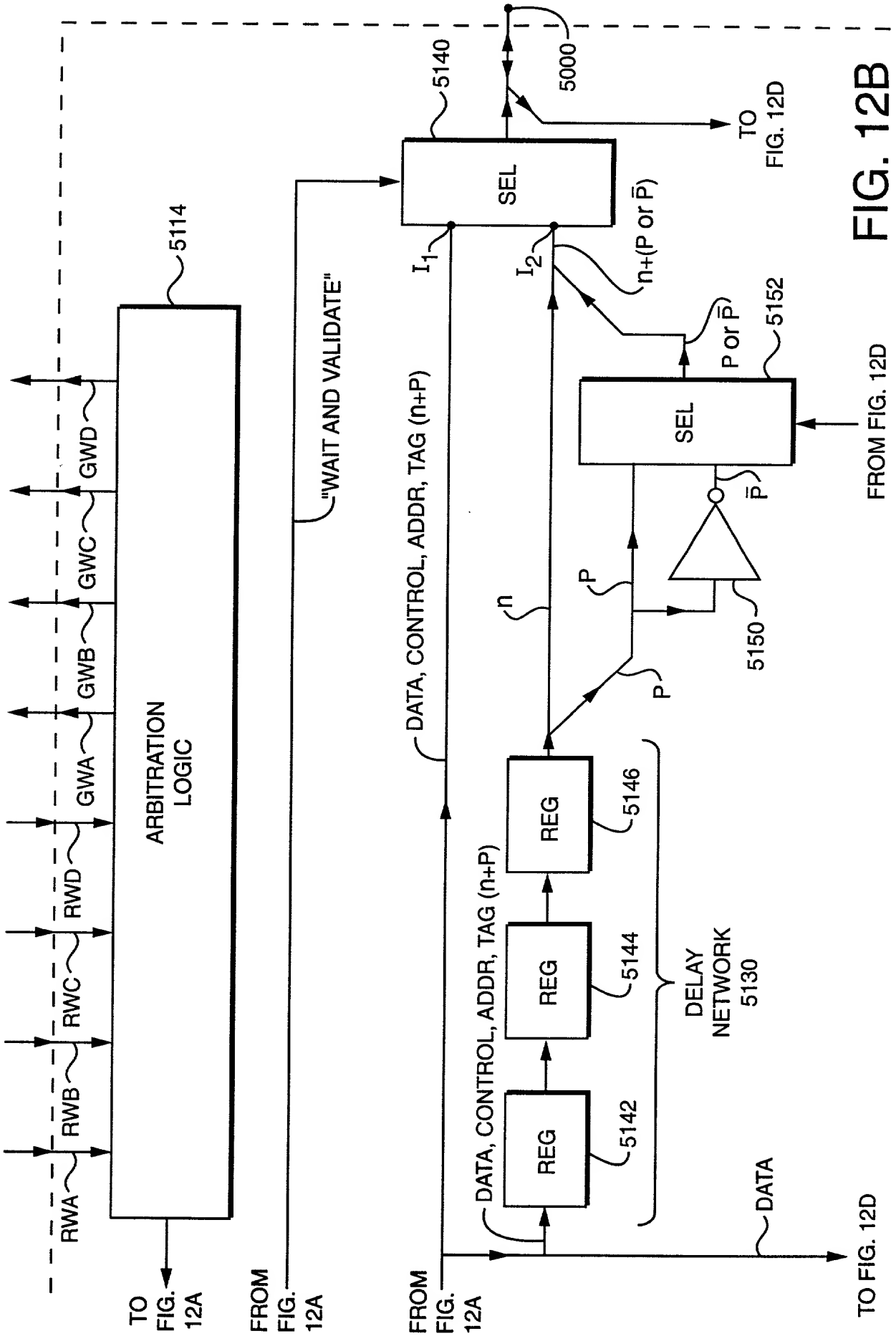

TO FIG. 12A
FROM FIG. 12A
RWA
RWB
RWC
RWD
GWA
GWB
GWC
GWD
ARBITRATION LOGIC
5114
"WAIT AND VALIDATE"
FROM FIG. 12A
DATA, CONTROL, ADDR, TAG (n+P)
SEL
5140
5000
TO FIG. 12D
I1
I2
n+(P or P̄)
P or P̄
5152
SEL
FROM FIG. 12D
P̄
5150
n
P
P
DATA, CONTROL, ADDR, TAG (n+P)
REG
5146
REG
5144
REG
5142
DELAY NETWORK 5130
DATA
TO FIG. 12D

FIG. 12B

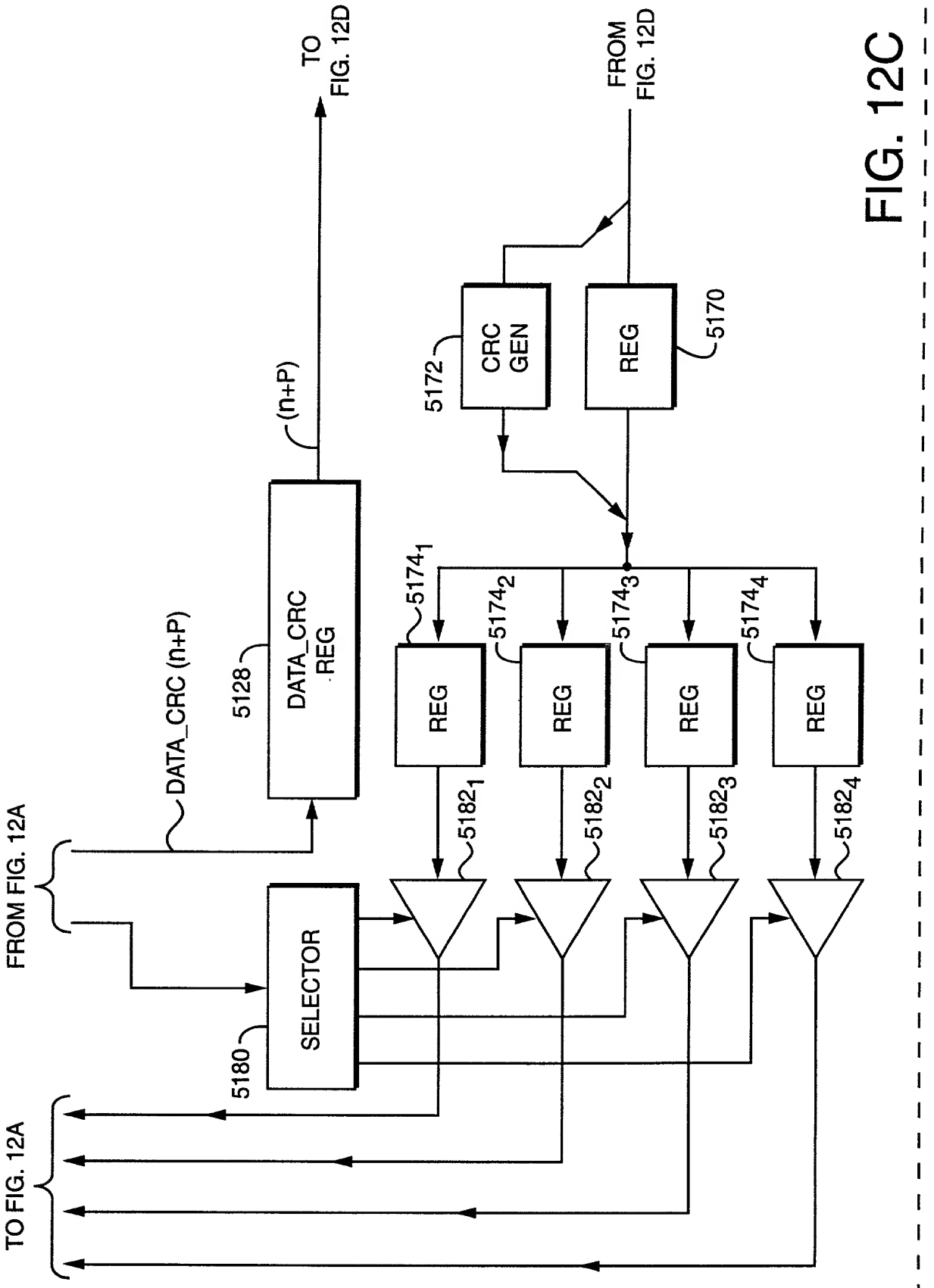

TO FIG. 12A
FROM FIG. 12A
SELECTOR
5180
DATA_CRC (n+P)
5128
DATA_CRC REG
(n+P)
TO FIG. 12D
FROM FIG. 12D
5172
CRC GEN
REG
5170
5174 1
5174 2
5174 3
5174 4
REG
REG
REG
REG
5182 1
5182 2
5182 3
5182 4

FIG. 12C

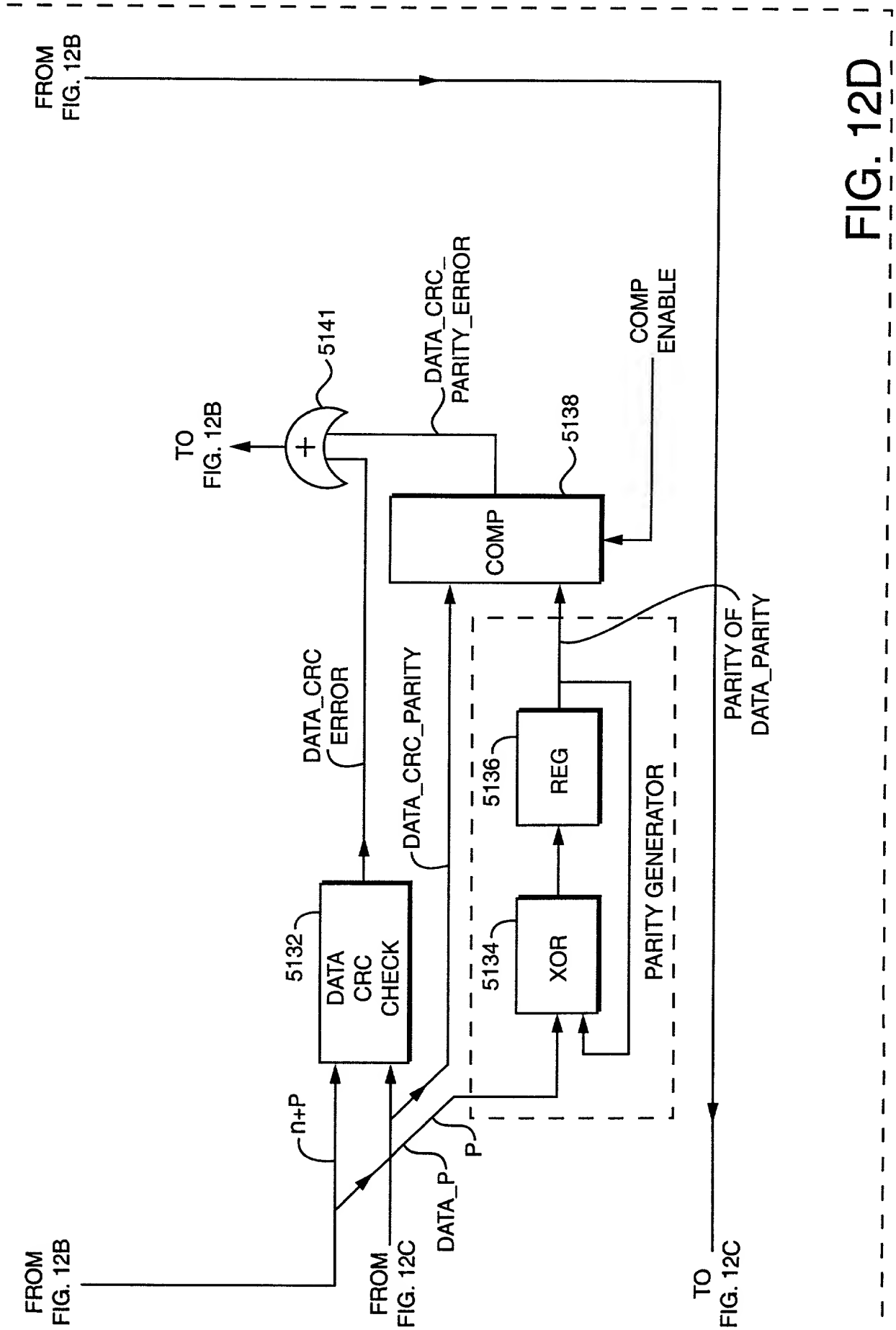

FROM FIG. 12B
TO FIG. 12B
5141
DATA_CRC_ PARITY_ERROR
COMP ENABLE
5138
COMP
DATA_CRC ERROR
DATA_CRC_PARITY
5136
REG
PARITY OF DATA_PARITY
PARITY GENERATOR
5132
DATA CRC CHECK
5134
XOR
n+P
P
DATA_P
FROM FIG. 12B
FROM FIG. 12C
TO FIG. 12C

FIG. 12D

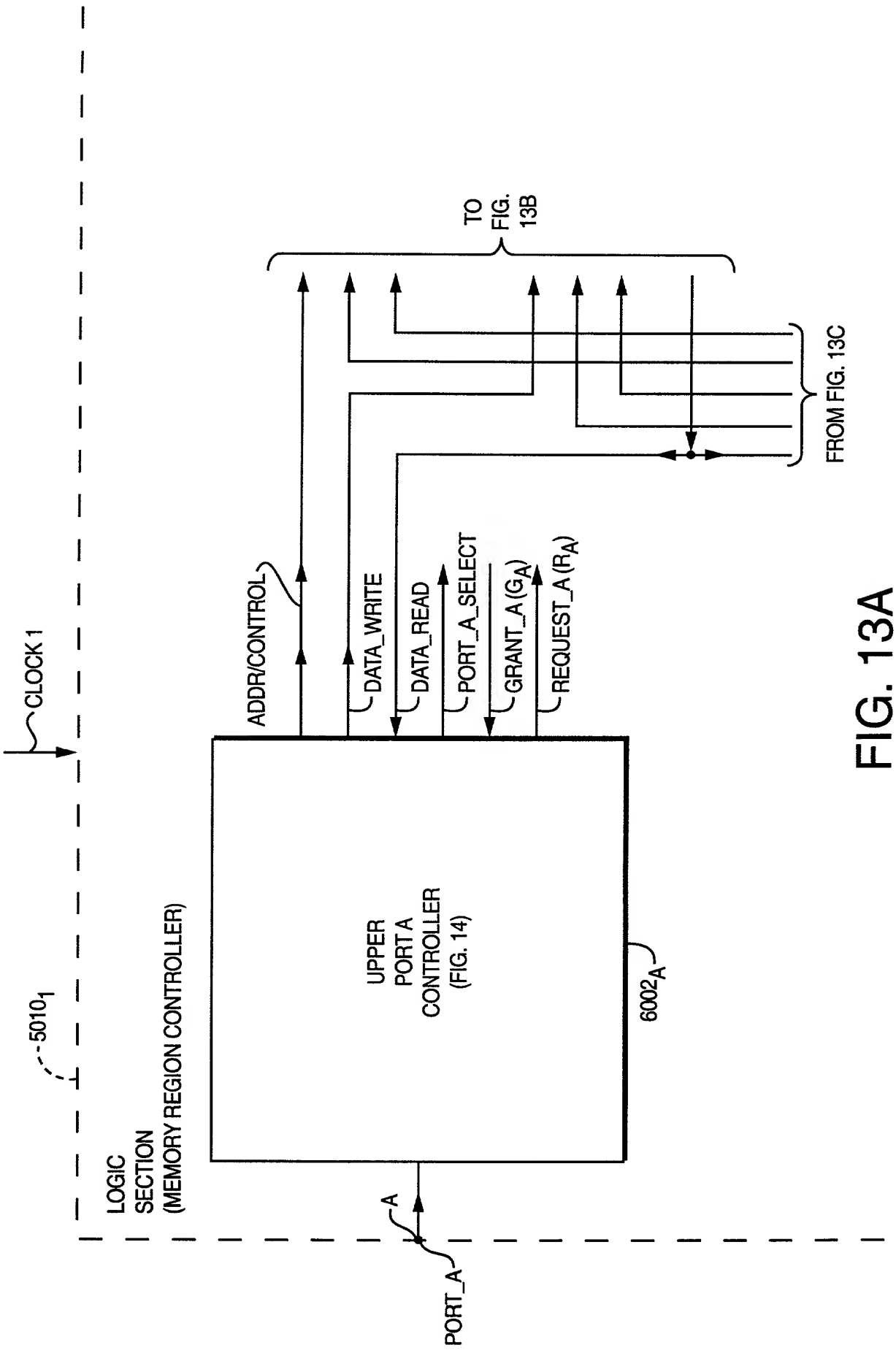

TO FIG. 13B
FROM FIG. 13C
ADDR/CONTROL
DATA_WRITE
DATA_READ
PORT_A_SELECT
GRANT_A (G_A)
REQUEST_A (R_A)
CLOCK 1
LOGIC SECTION (MEMORY REGION CONTROLLER)
5010_1
UPPER PORT A CONTROLLER (FIG. 14)
6002_A
A
PORT_A

FIG. 13A

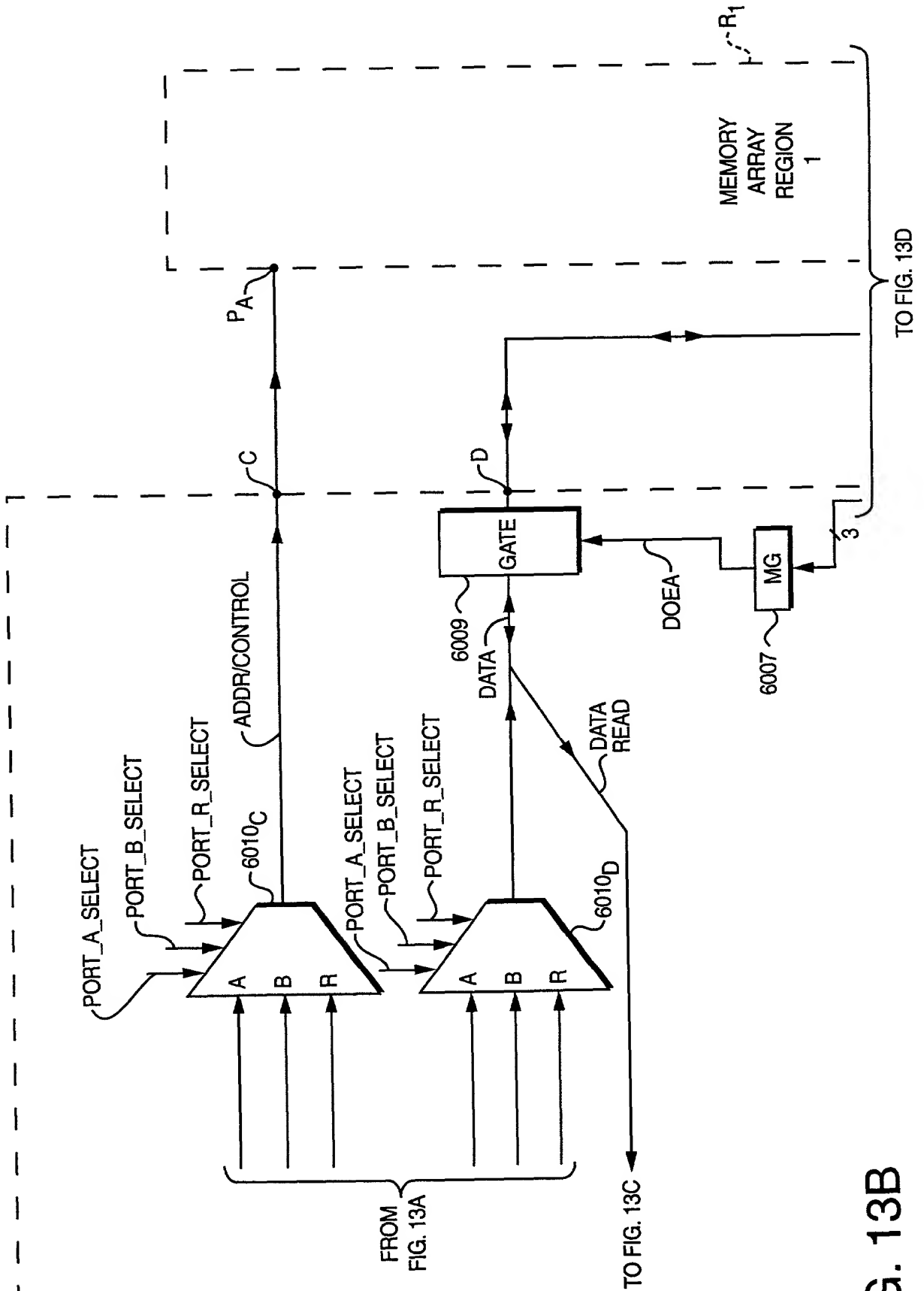

MEMORY ARRAY REGION 1
R_1
TO FIG. 13D
P_A
C
D
GATE
6009
DATA
DOEA
MG
6007
3
ADDR/CONTROL
PORT_A_SELECT
PORT_B_SELECT
PORT_R_SELECT
6010_C
PORT_A_SELECT
PORT_B_SELECT
PORT_R_SELECT
6010_D
DATA READ
A
B
R
A
B
R
FROM FIG. 13A
TO FIG. 13C

FIG. 13B

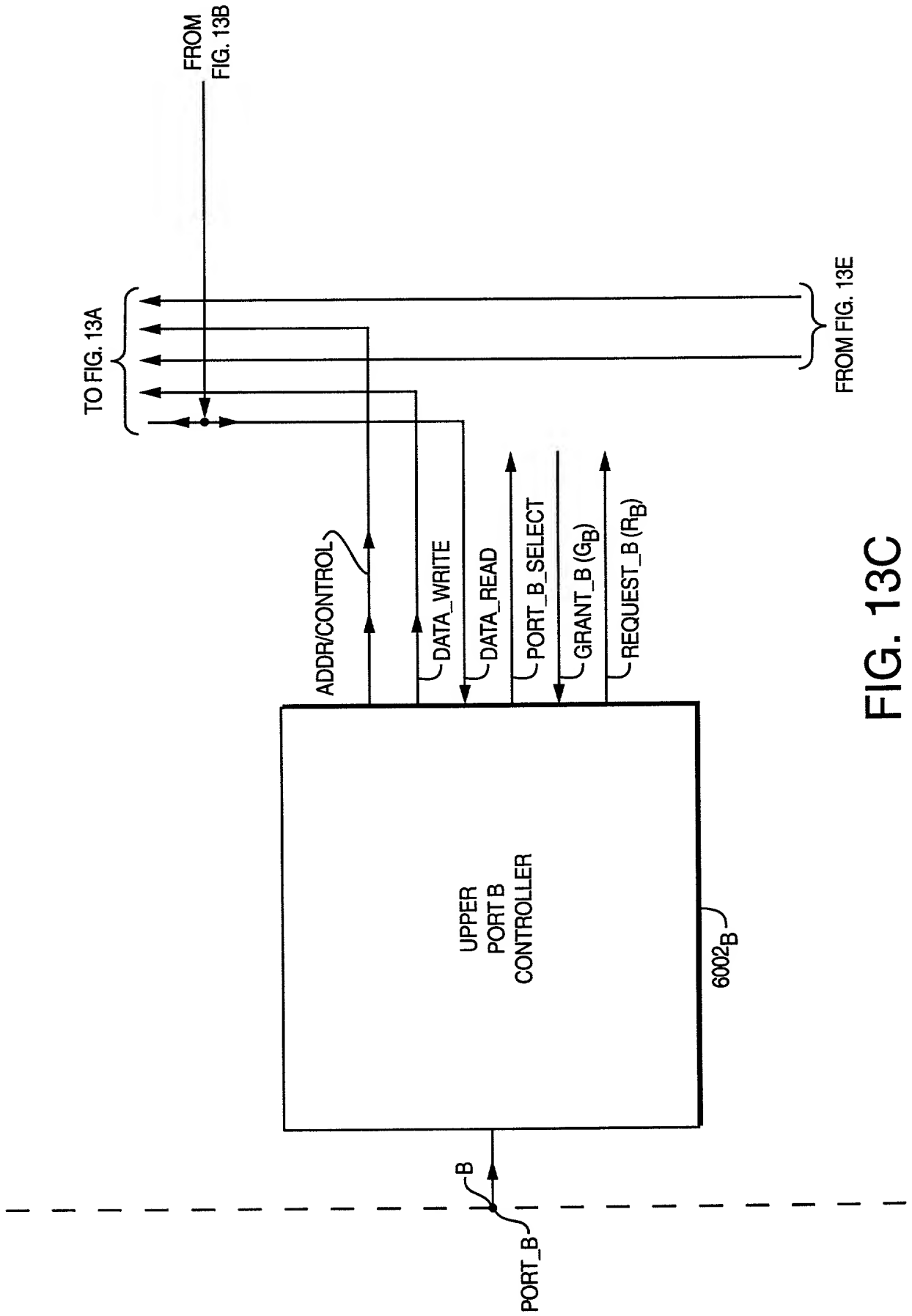

FROM FIG. 13B
TO FIG. 13A
FROM FIG. 13E
ADDR/CONTROL
DATA_WRITE
DATA_READ
PORT_B_SELECT
GRANT_B (G_B)
REQUEST_B (R_B)
UPPER PORT B CONTROLLER
6002_B
B
PORT_B

FIG. 13C

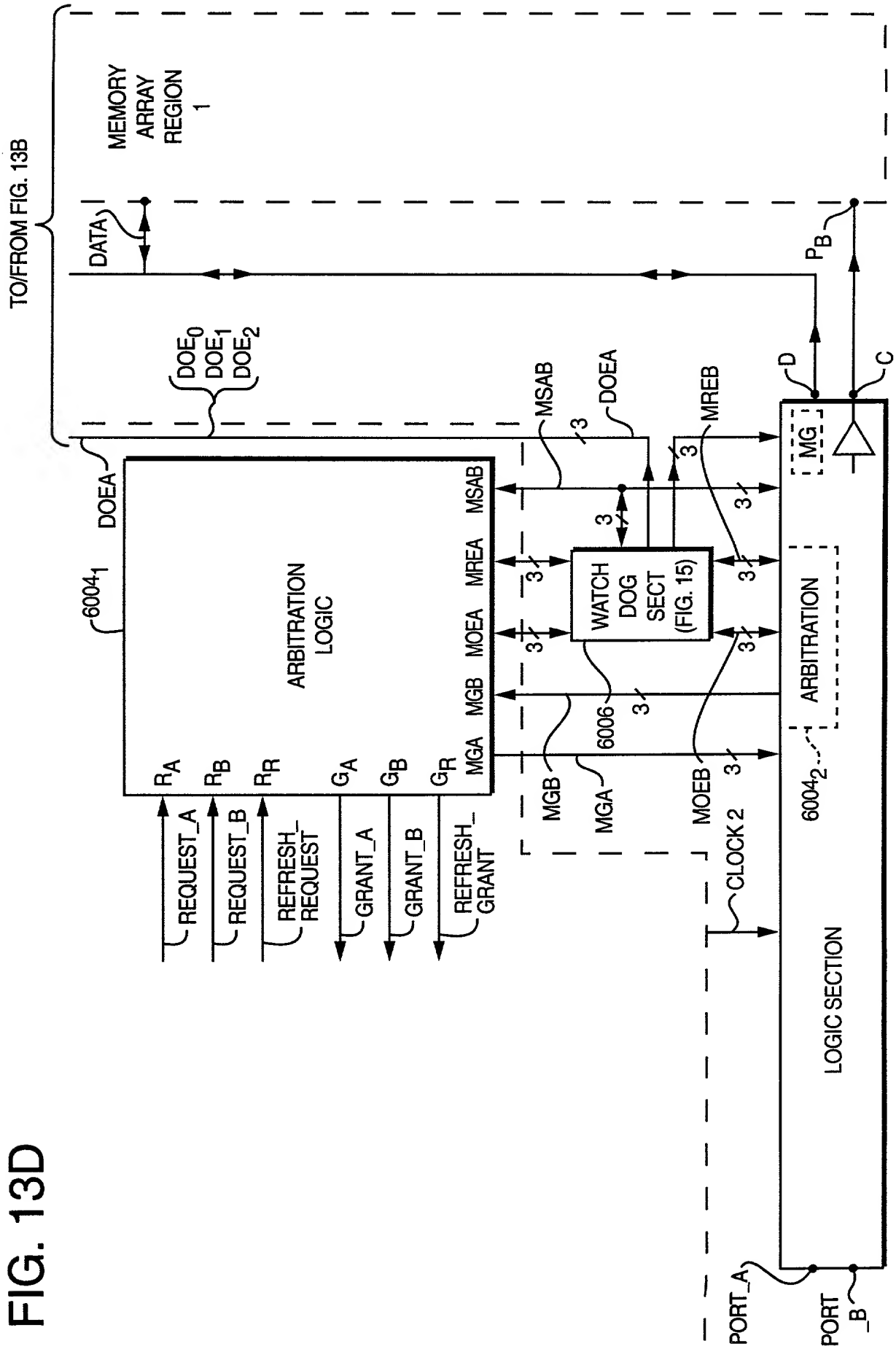

TO/FROM FIG. 13B
MEMORY ARRAY REGION 1
DATA
DOE_0 DOE_1 DOE_2
DOEA
6004_1
ARBITRATION LOGIC
MSAB
MREA
MOEA
MGB
MGA
R_A R_B R_R G_A G_B G_R
REQUEST_A
REQUEST_B
REFRESH_ REQUEST
GRANT_A
GRANT_B
REFRESH_ GRANT
WATCH DOG SECT (FIG. 15)
6006
MOEB
CLOCK 2
P_B
D
C
MG
ARBITRATION
6004_2
LOGIC SECTION
PORT_A
PORT _B

FIG. 13D

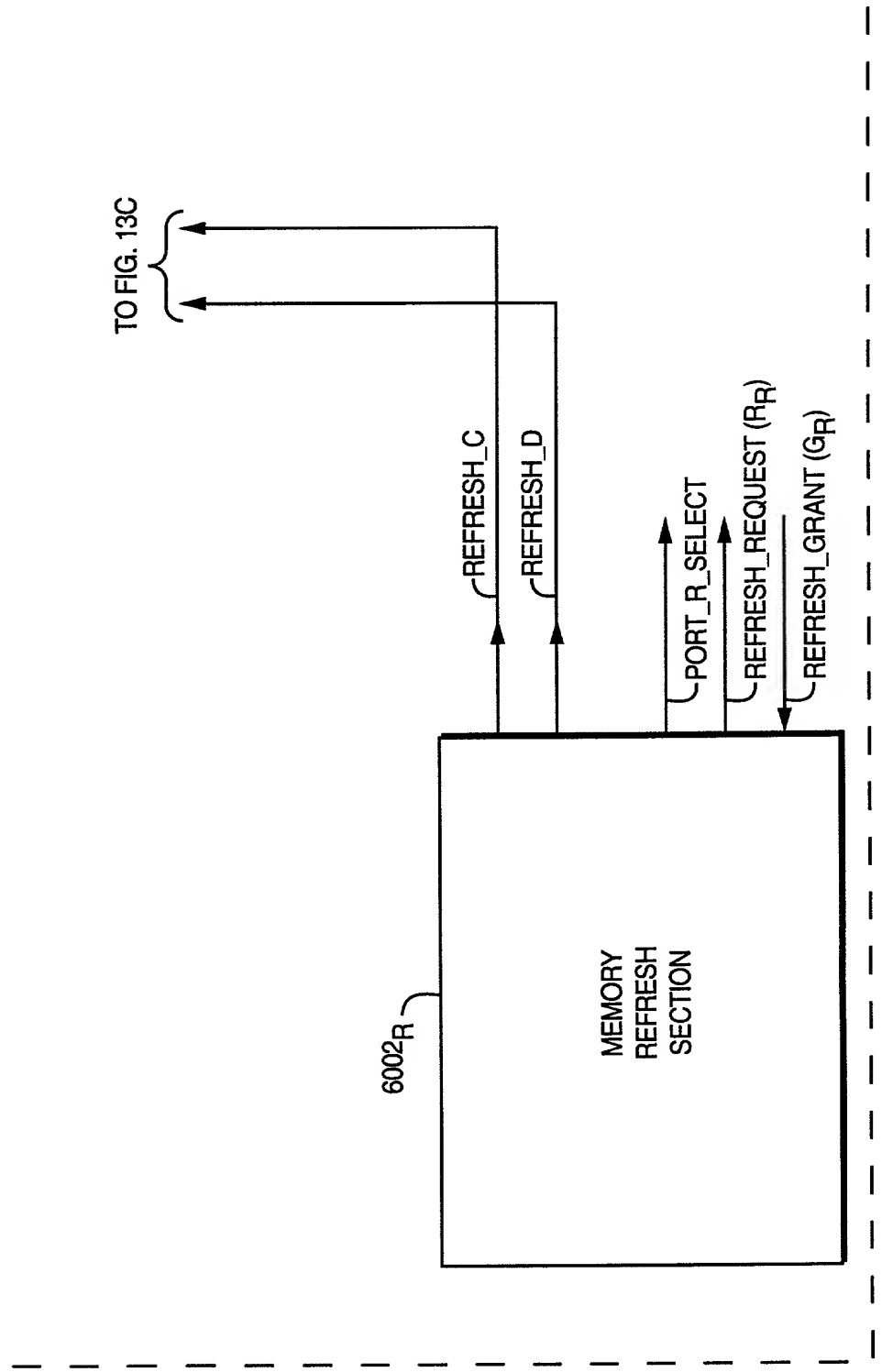

TO FIG. 13C
REFRESH_C
REFRESH_D
PORT_R_SELECT
REFRESH_REQUEST (R_R)
REFRESH_GRANT (G_R)
6002_R
MEMORY
REFRESH
SECTION

FIG. 13E

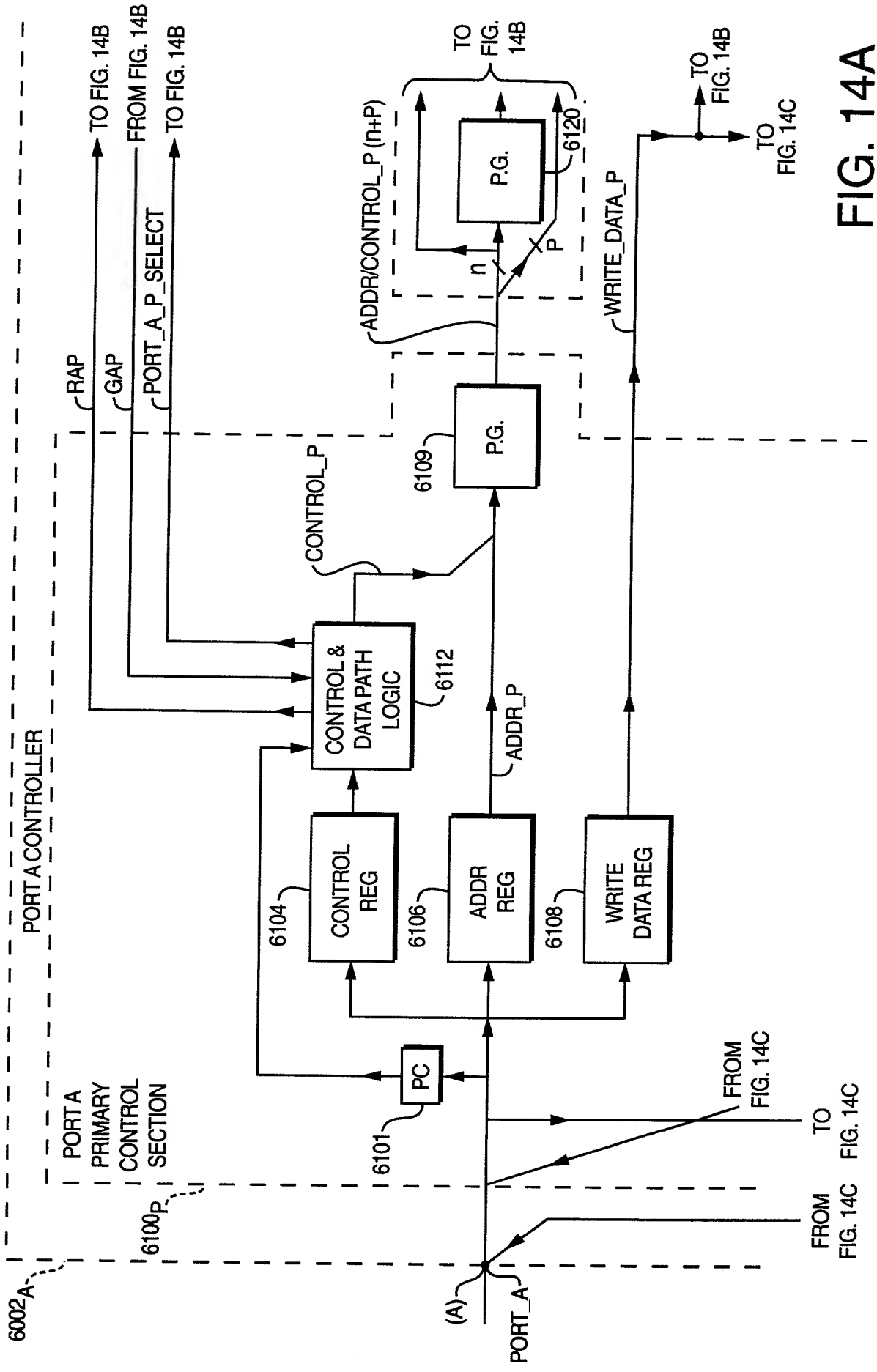

6002A
PORT A CONTROLLER
PORT A PRIMARY CONTROL SECTION
6100P
PORT_A
(A)
PC
6101
CONTROL REG
6104
ADDR REG
6106
WRITE DATA REG
6108
CONTROL & DATA PATH LOGIC
6112
P.G.
6109
P.G.
6120
P
n
ADDR_P
CONTROL_P
ADDR/CONTROL_P (n+P)
WRITE_DATA_P
RAP
GAP
PORT_A_P_SELECT
TO FIG. 14B
FROM FIG. 14B
TO FIG. 14B
TO FIG. 14B
TO FIG. 14B
TO FIG. 14C
FROM FIG. 14C
TO FIG. 14C
FROM FIG. 14C

FIG. 14A

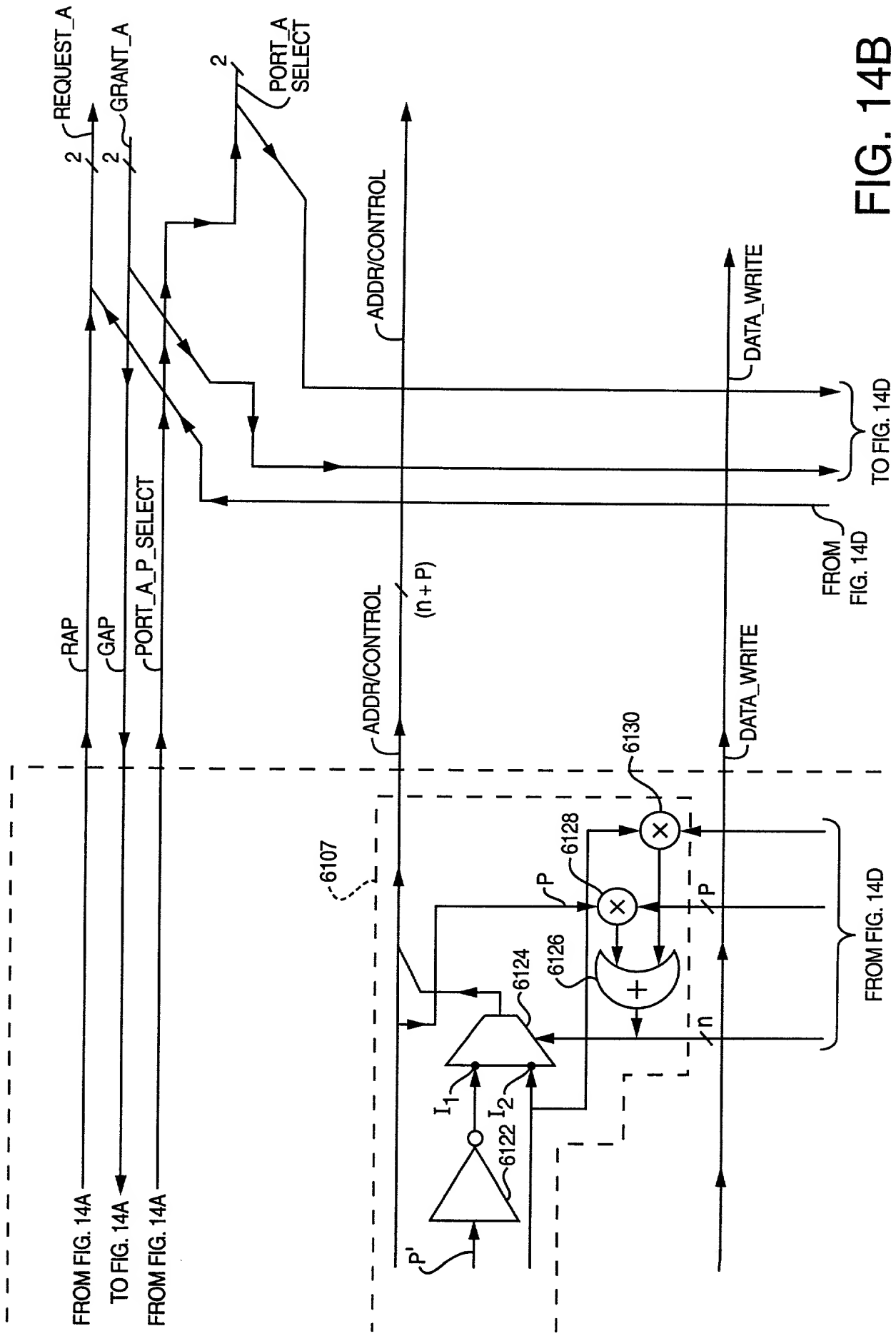

REQUEST_A
GRANT_A
PORT_A SELECT
2
2
2
ADDR/CONTROL
DATA_WRITE
TO FIG. 14D
FROM FIG. 14D
RAP
GAP
PORT_A_P_SELECT
ADDR/CONTROL
(n+P)
DATA_WRITE
6130
6128
6107
P
P
6124
6126
n
FROM FIG. 14D
I_1
I_2
6122
P'
FROM FIG. 14A
TO FIG. 14A
FROM FIG. 14A

FIG. 14B

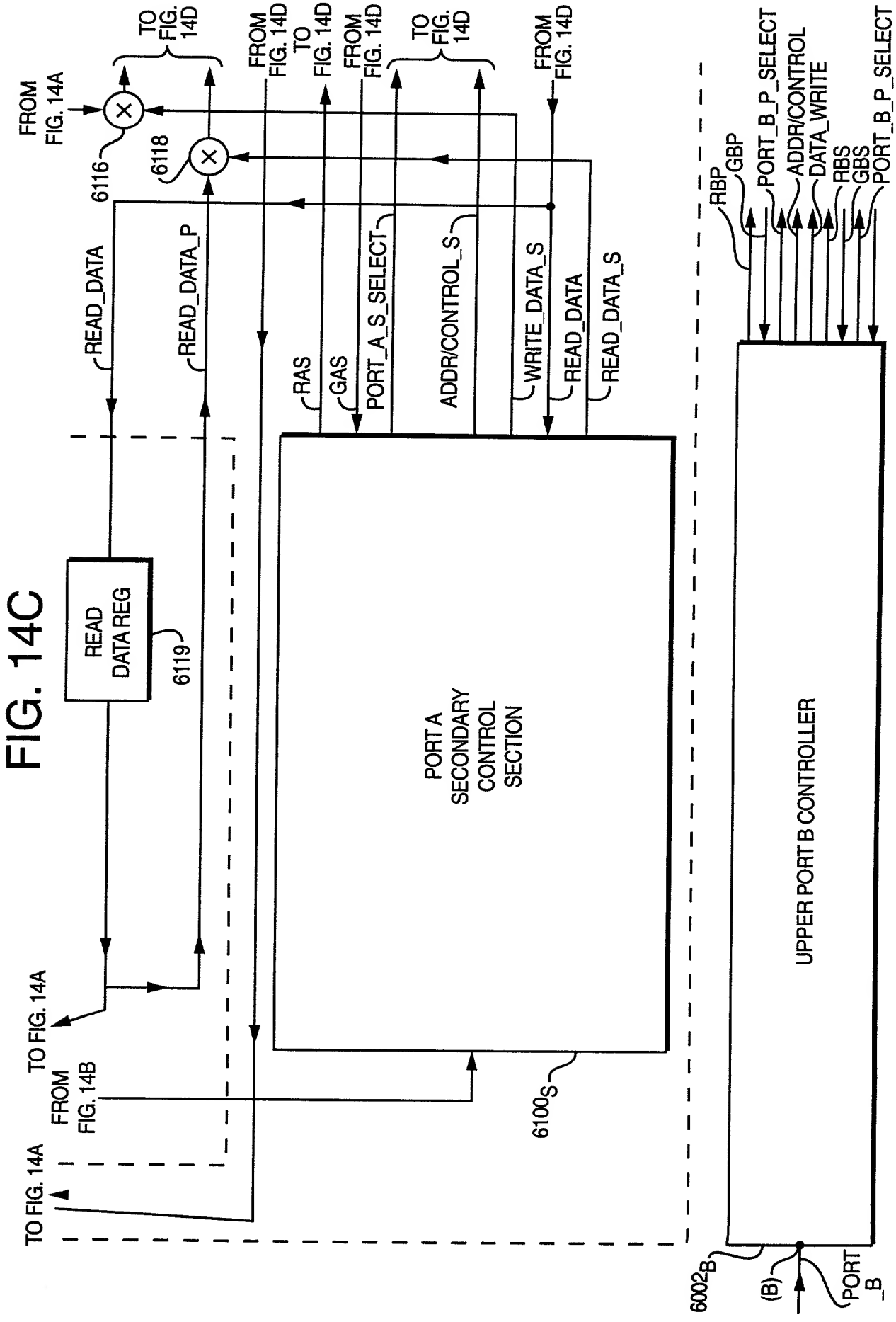

FROM FIG. 14A
6116
6118
TO FIG. 14D
FROM FIG. 14D
TO FIG. 14D
FROM FIG. 14D
TO FIG. 14D
FROM FIG. 14D
READ_DATA
READ_DATA_P
RAS
GAS
PORT_A_S_SELECT
ADDR/CONTROL_S
WRITE_DATA_S
READ_DATA
READ_DATA_S
RBP
GBP
PORT_B_P_SELECT
ADDR/CONTROL
DATA_WRITE
RBS
GBS
PORT_B_P_SELECT
READ DATA REG
6119
PORT A SECONDARY CONTROL SECTION
UPPER PORT B CONTROLLER
TO FIG. 14A
FROM FIG. 14B
TO FIG. 14A
6100S
6002B
(B)
PORT B

FIG. 14C

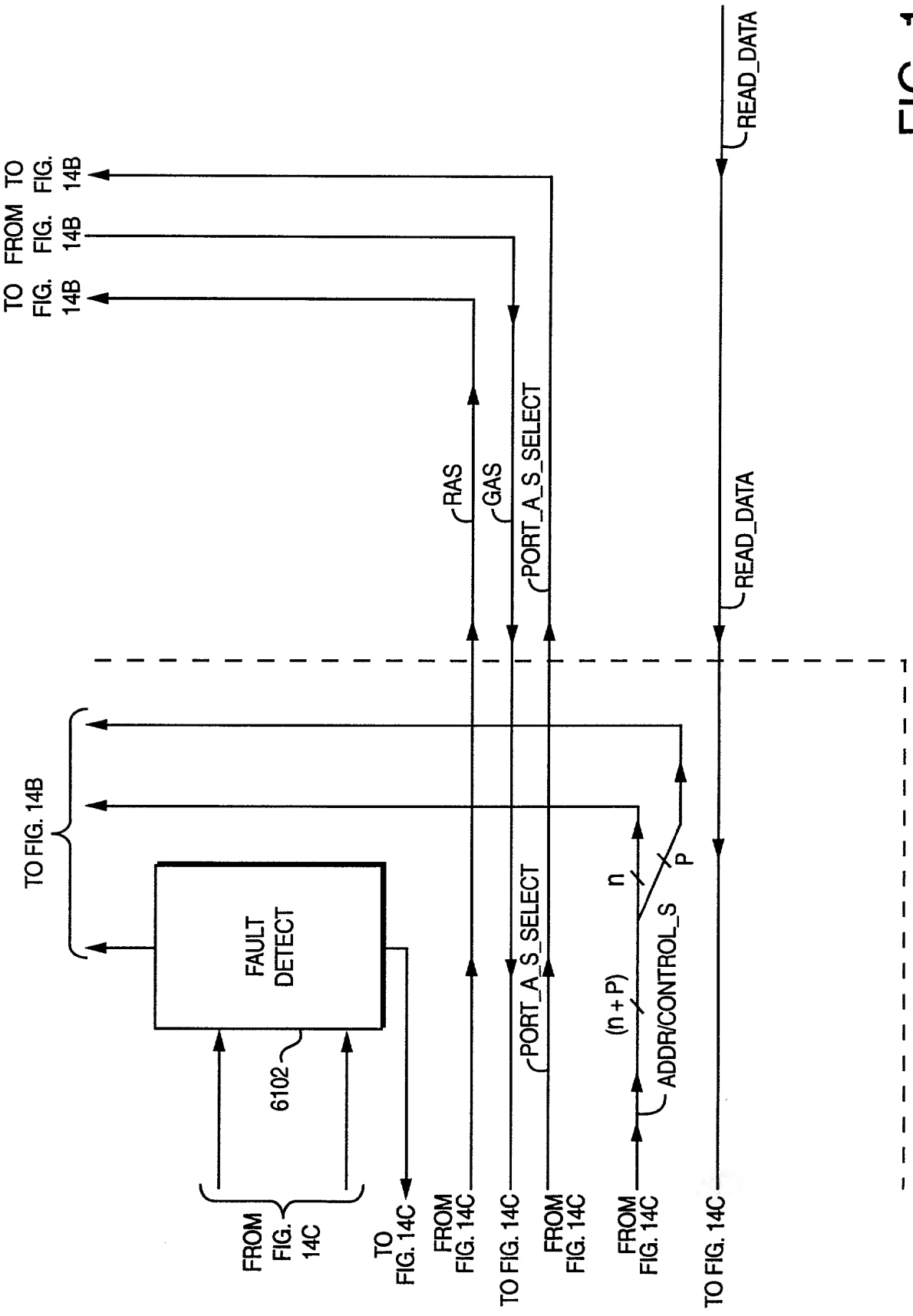

TO FIG. 14B
FROM FIG. 14B
TO FIG. 14B
READ_DATA
RAS
GAS
PORT_A_S_SELECT
READ_DATA
TO FIG. 14B
FAULT DETECT
6102
FROM FIG. 14C
TO FIG. 14C
FROM FIG. 14C
TO FIG. 14C
PORT_A_S_SELECT
FROM FIG. 14C
(n+P)
n
P
ADDR/CONTROL_S
TO FIG. 14C

FIG. 14D

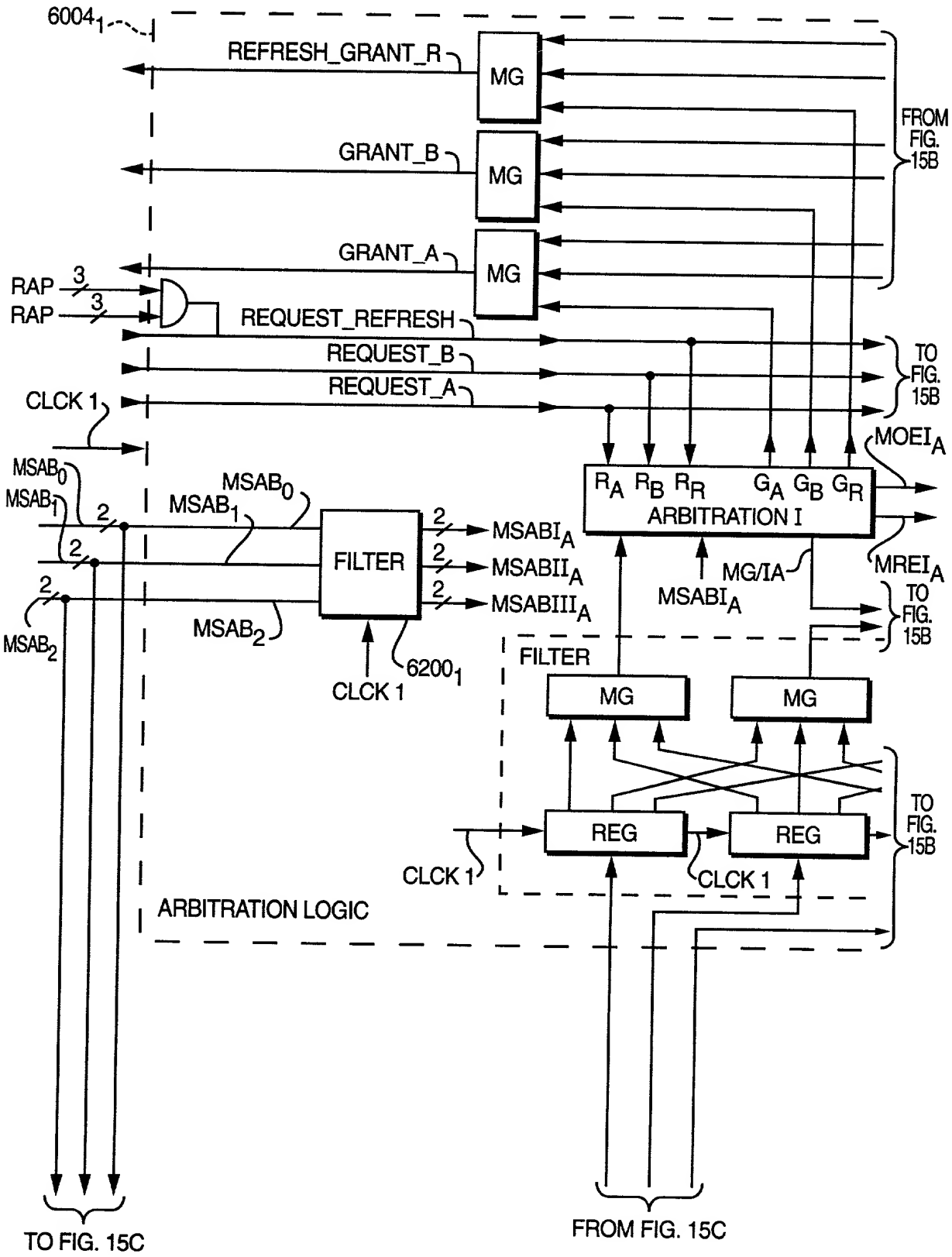

6004 1
REFRESH_GRANT_R
MG
GRANT_B
MG
GRANT_A
MG
FROM FIG. 15B
RAP 3
RAP 3
REQUEST_REFRESH
REQUEST_B
REQUEST_A
TO FIG. 15B
CLCK 1
MOEI A
MSAB 0
MSAB 1
MSAB 2
2
FILTER
MSABI A
MSABII A
MSABIII A
6200 1
CLCK 1
R A R B R R G A G B G R
ARBITRATION I
MG/IA
MSABI A
MREI A
TO FIG. 15B
FILTER
MG
MG
REG
REG
CLCK 1
CLCK 1
TO FIG. 15B
ARBITRATION LOGIC
TO FIG. 15C
FROM FIG. 15C

FIG. 15A

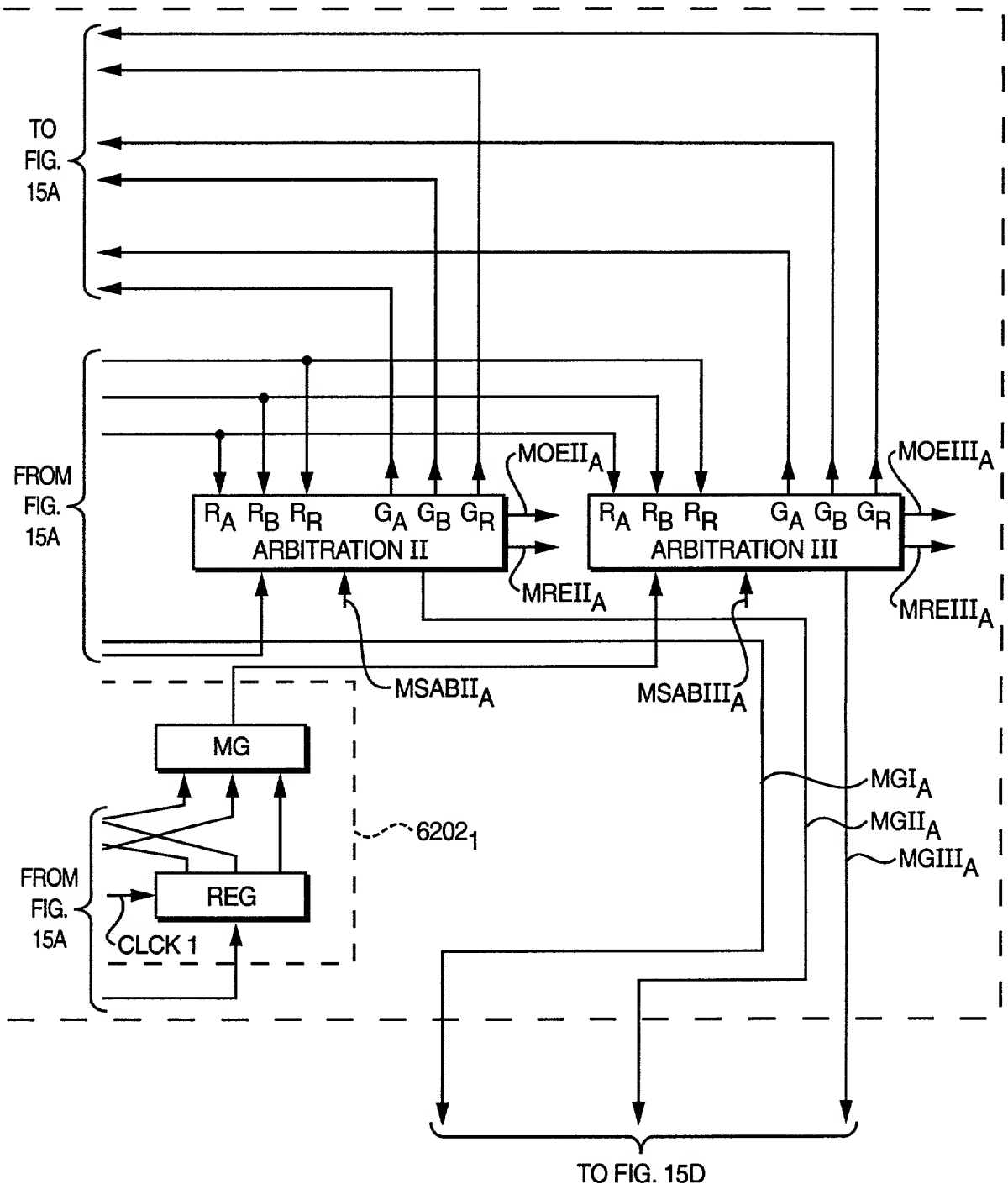

TO
FIG.
15A
FROM
FIG.
15A
R_A R_B R_R G_A G_B G_R
ARBITRATION II
R_A R_B R_R G_A G_B G_R
ARBITRATION III
$MOEII_A$
$MOEIII_A$
$MREII_A$
$MREIII_A$
$MSABII_A$
$MSABIII_A$
MG
REG
CLCK 1
6202_1
FROM
FIG.
15A
MGI_A
$MGII_A$
$MGIII_A$
TO FIG. 15D

FIG. 15B

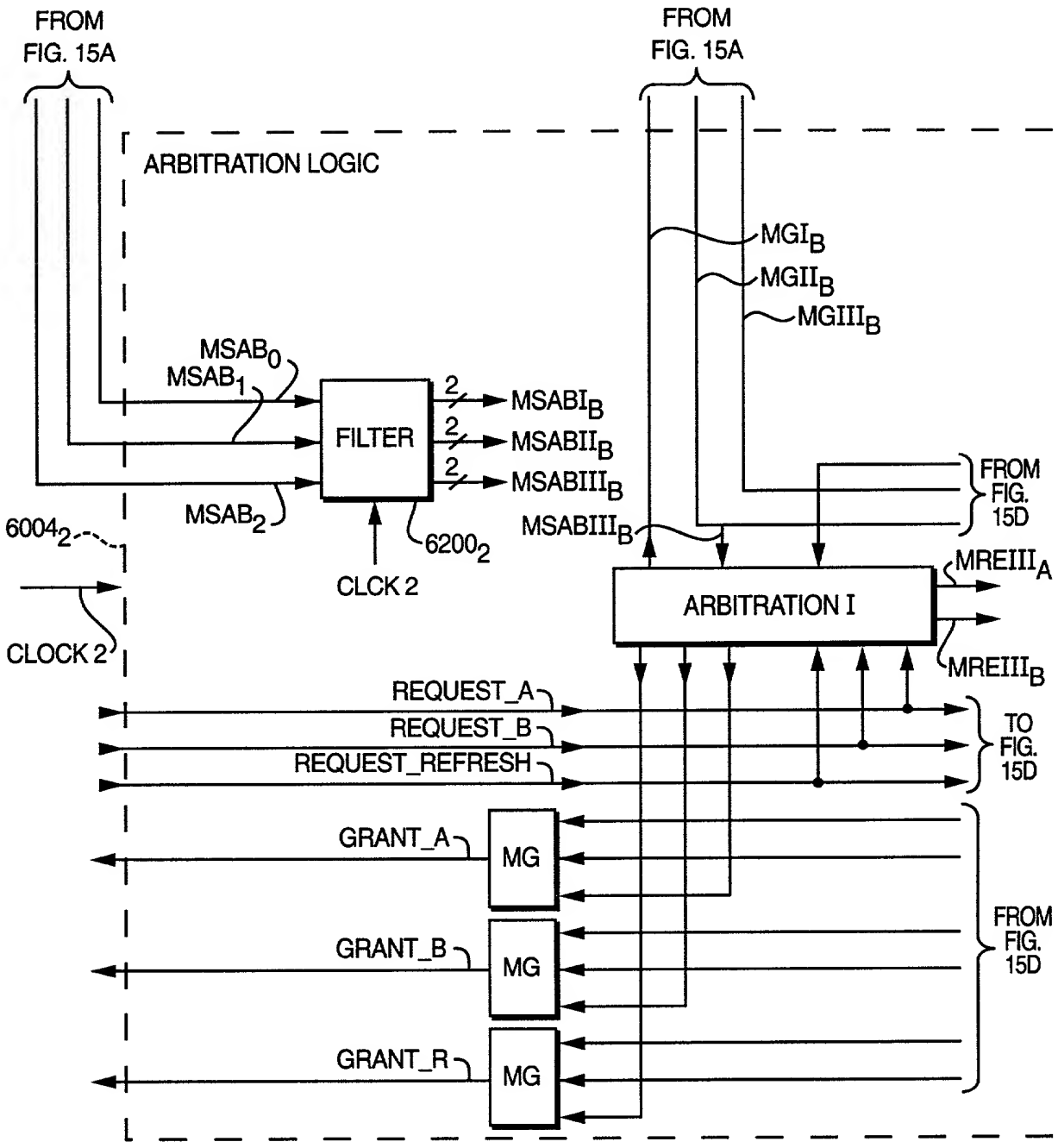

FROM
FIG. 15A
FROM
FIG. 15A
ARBITRATION LOGIC
MGI$_B$
MGII$_B$
MGIII$_B$
MSAB$_0$
MSAB$_1$
FILTER
2
2
2
MSABI$_B$
MSABII$_B$
MSABIII$_B$
MSAB$_2$
6004$_2$
6200$_2$
CLCK 2
MSABIII$_B$
FROM
FIG.
15D
MREIII$_A$
ARBITRATION I
MREIII$_B$
CLOCK 2
REQUEST_A
REQUEST_B
REQUEST_REFRESH
TO
FIG.
15D
GRANT_A
MG
GRANT_B
MG
GRANT_R
MG
FROM
FIG.
15D

FIG. 15C

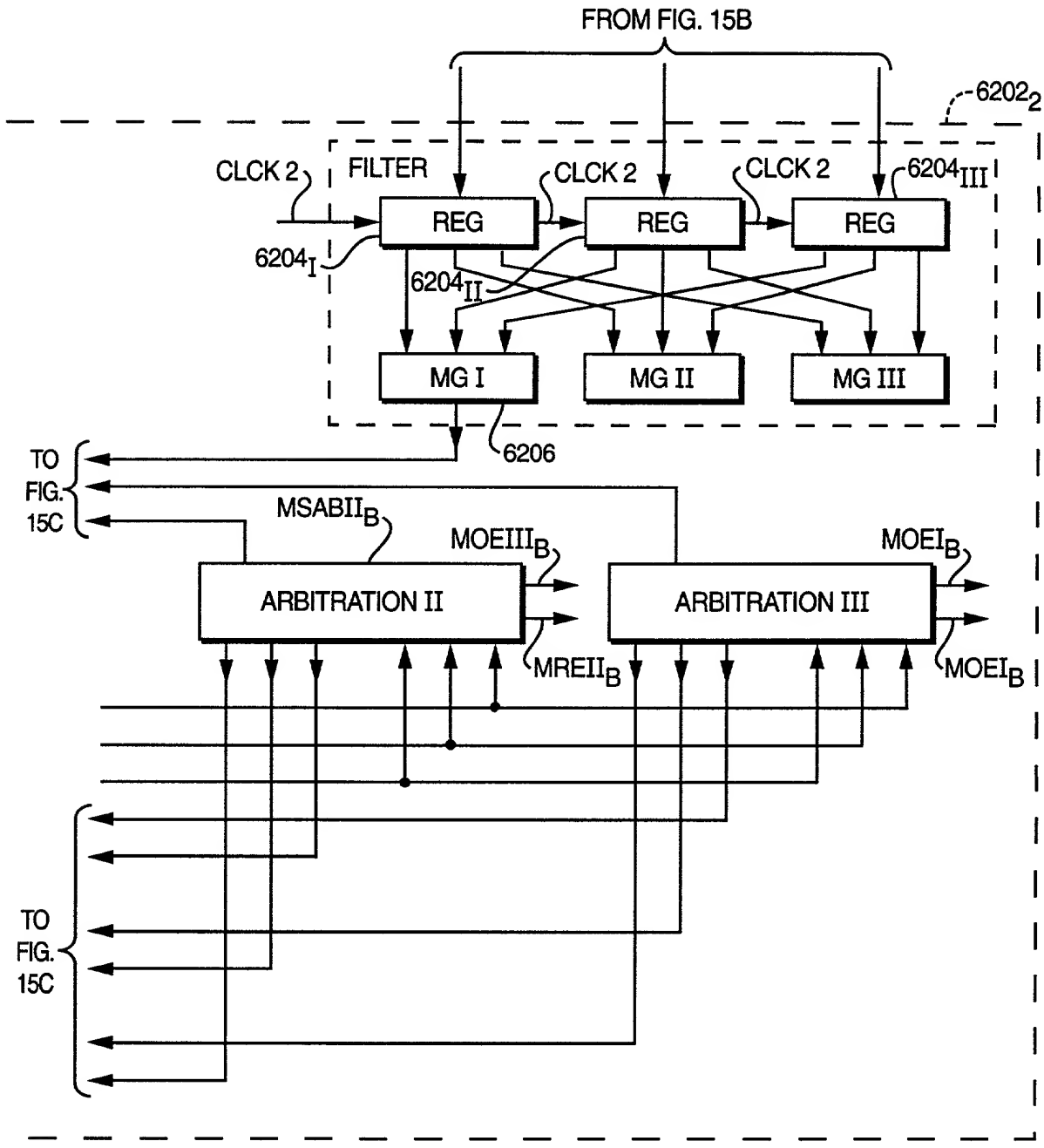

FROM FIG. 15B
6202$_2$
CLCK 2
FILTER
CLCK 2
CLCK 2
6204$_{III}$
REG
REG
REG
6204$_I$
6204$_{II}$
MG I
MG II
MG III
6206
TO FIG. 15C
MSABII$_B$
MOEIII$_B$
MOEI$_B$
ARBITRATION II
ARBITRATION III
MREII$_B$
MOEI$_B$
TO FIG. 15C

FIG. 15D

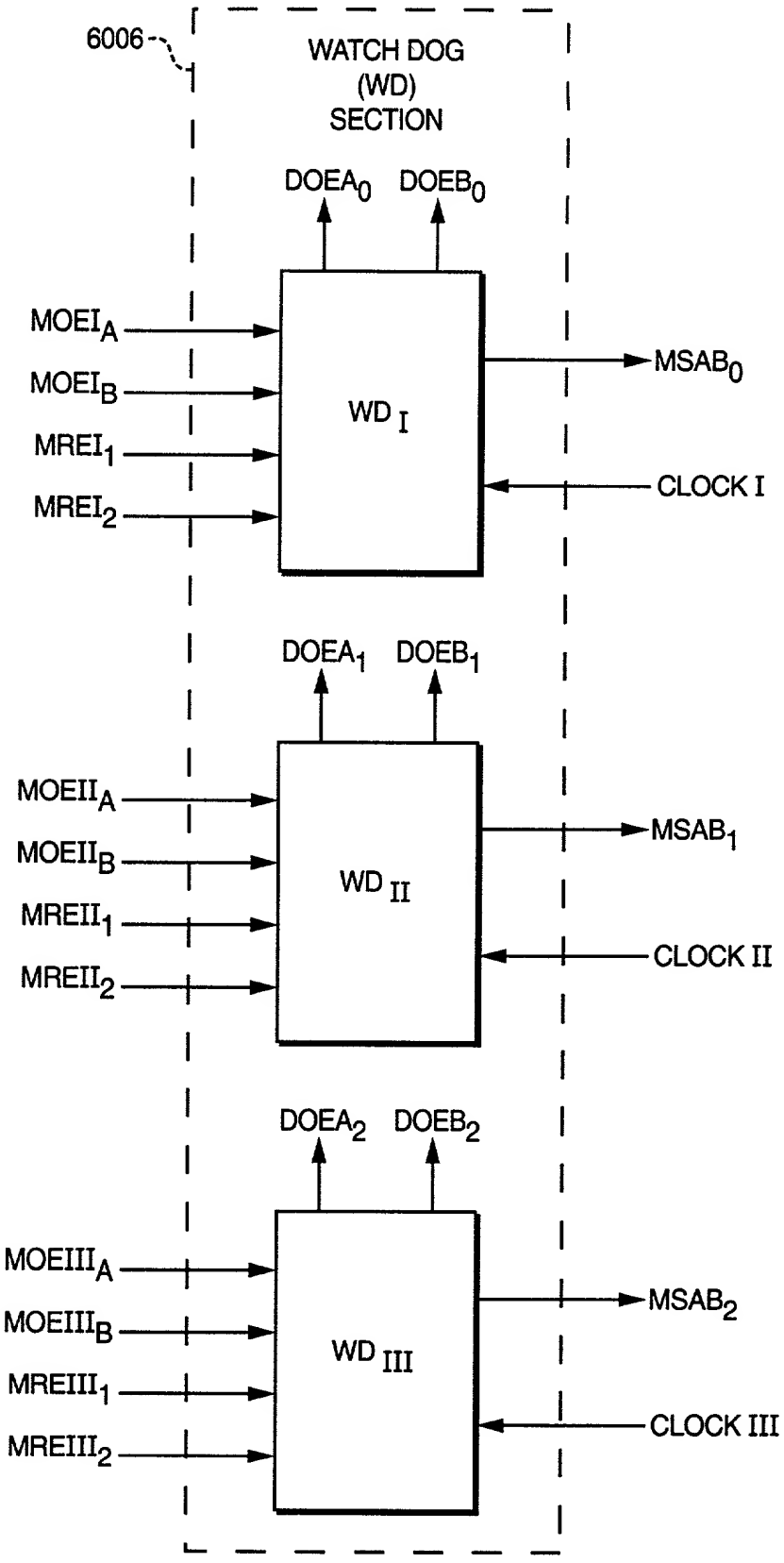

6006
WATCH DOG
(WD)
SECTION
DOEA0
DOEB0
MOEIA
MOEIB
MREI1
MREI2
WD I
MSAB0
CLOCK I
DOEA1
DOEB1
MOEIIA
MOEIIB
MREII1
MREII2
WD II
MSAB1
CLOCK II
DOEA2
DOEB2
MOEIIIA
MOEIIIB
MREIII1
MREIII2
WD III
MSAB2
CLOCK III

FIG. 15E

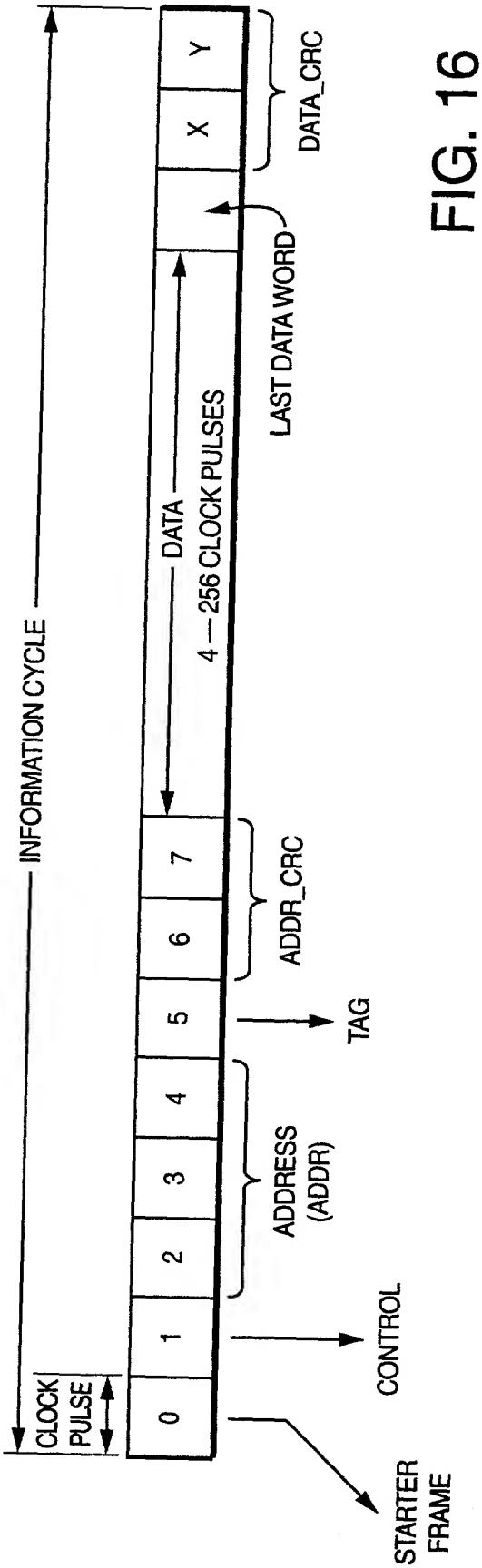


FIG. 16

MG INPUTS	MG OUTPUT	MG OUTPUT	MG OUTPUT
000	0	0	0
001	0	0	0
010	0	0	0
011	1	1	1
100	0	0	0
101	1	1	1
110	1	1	1
111	1	1	1

FIG. 17

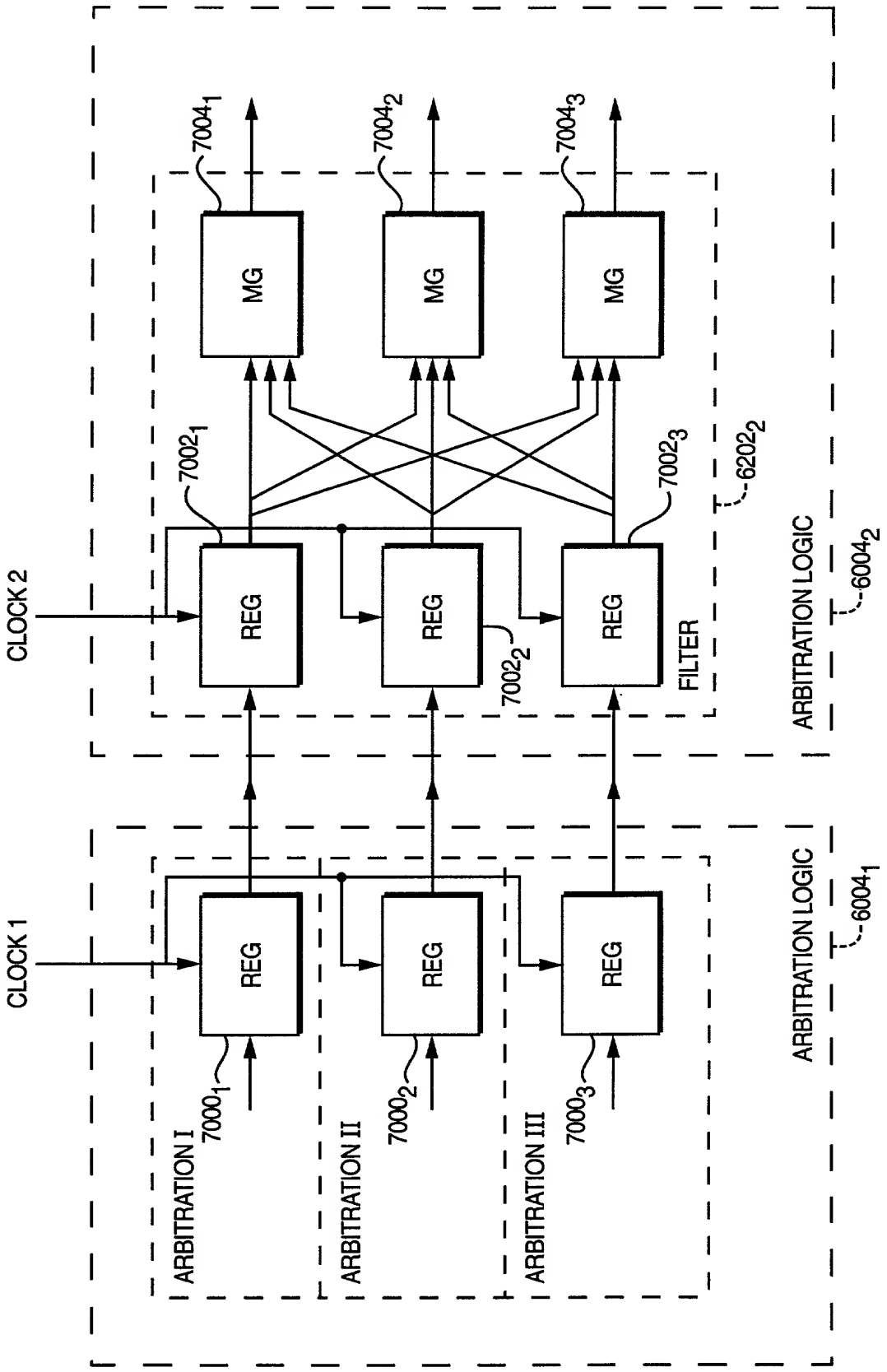

CLOCK 2
CLOCK 1
REG
REG
REG
REG
REG
REG
MG
MG
MG
7004_1
7004_2
7004_3
7002_1
7002_2
7002_3
6202_2
FILTER
ARBITRATION LOGIC
6004_2
ARBITRATION LOGIC
6004_1
ARBITRATION I
ARBITRATION II
ARBITRATION III
7000_1
7000_2
7000_3

FIG. 18

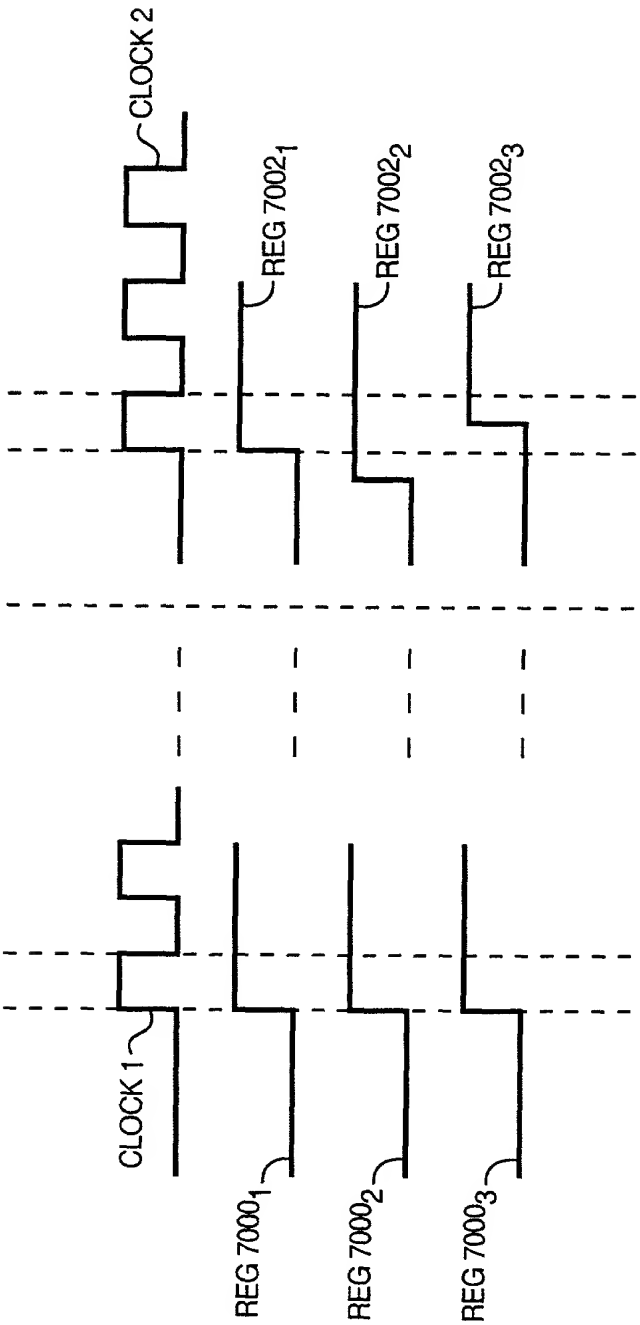

CLOCK 2
REG 7002$_1$
REG 7002$_2$
REG 7002$_3$
CLOCK 1
REG 7000$_1$
REG 7000$_2$
REG 7000$_3$

FIG. 19

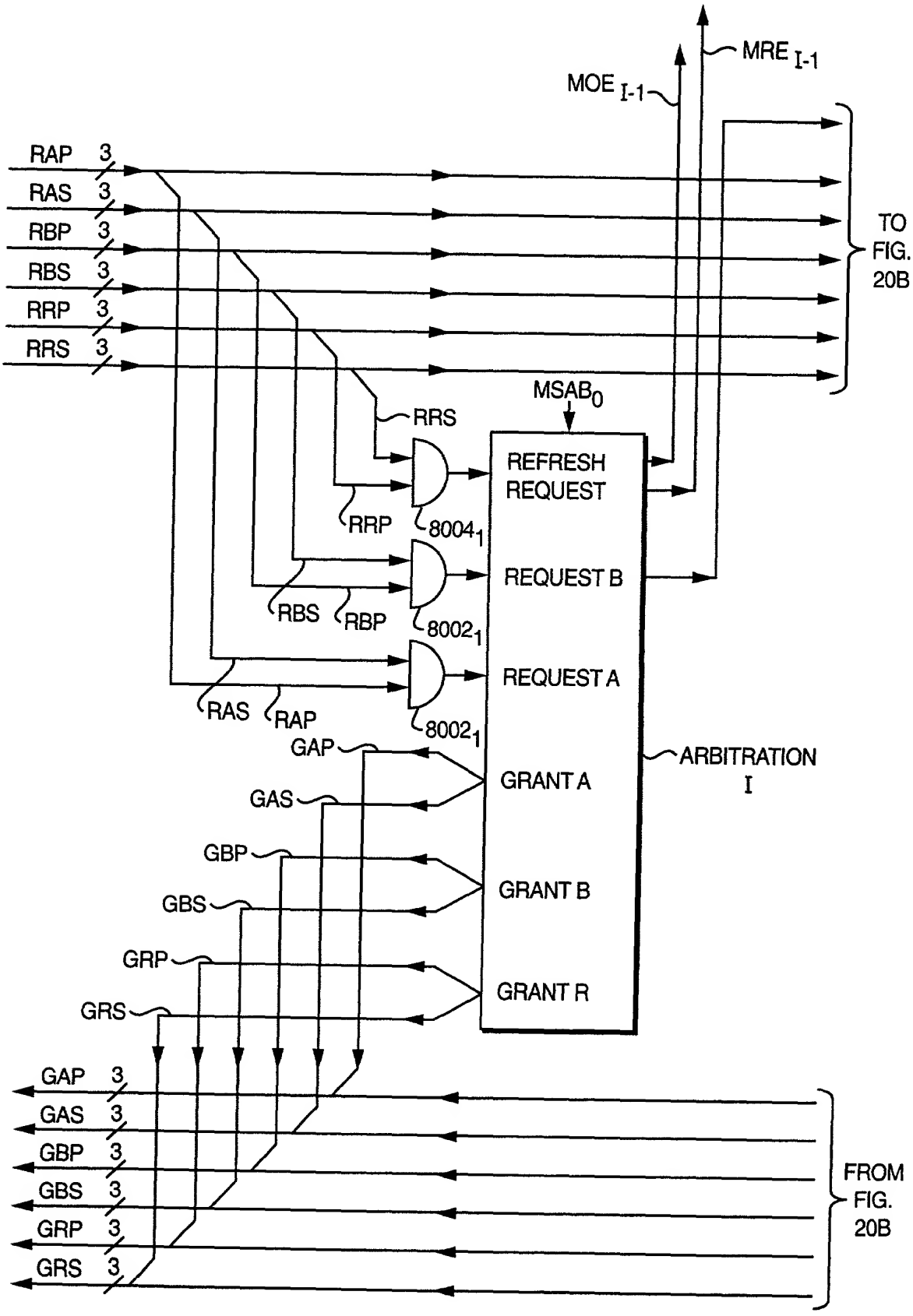

MOE I-1
MRE I-1
RAP 3
RAS 3
RBP 3
RBS 3
RRP 3
RRS 3
TO FIG. 20B
MSAB0
RRS
RRP
8004 1
REFRESH REQUEST
REQUEST B
RBS
RBP
8002 1
REQUEST A
RAS
RAP
8002 1
GAP
GAS
GRANT A
ARBITRATION I
GBP
GBS
GRANT B
GRP
GRS
GRANT R
GAP 3
GAS 3
GBP 3
GBS 3
GRP 3
GRS 3
FROM FIG. 20B

FIG. 20A

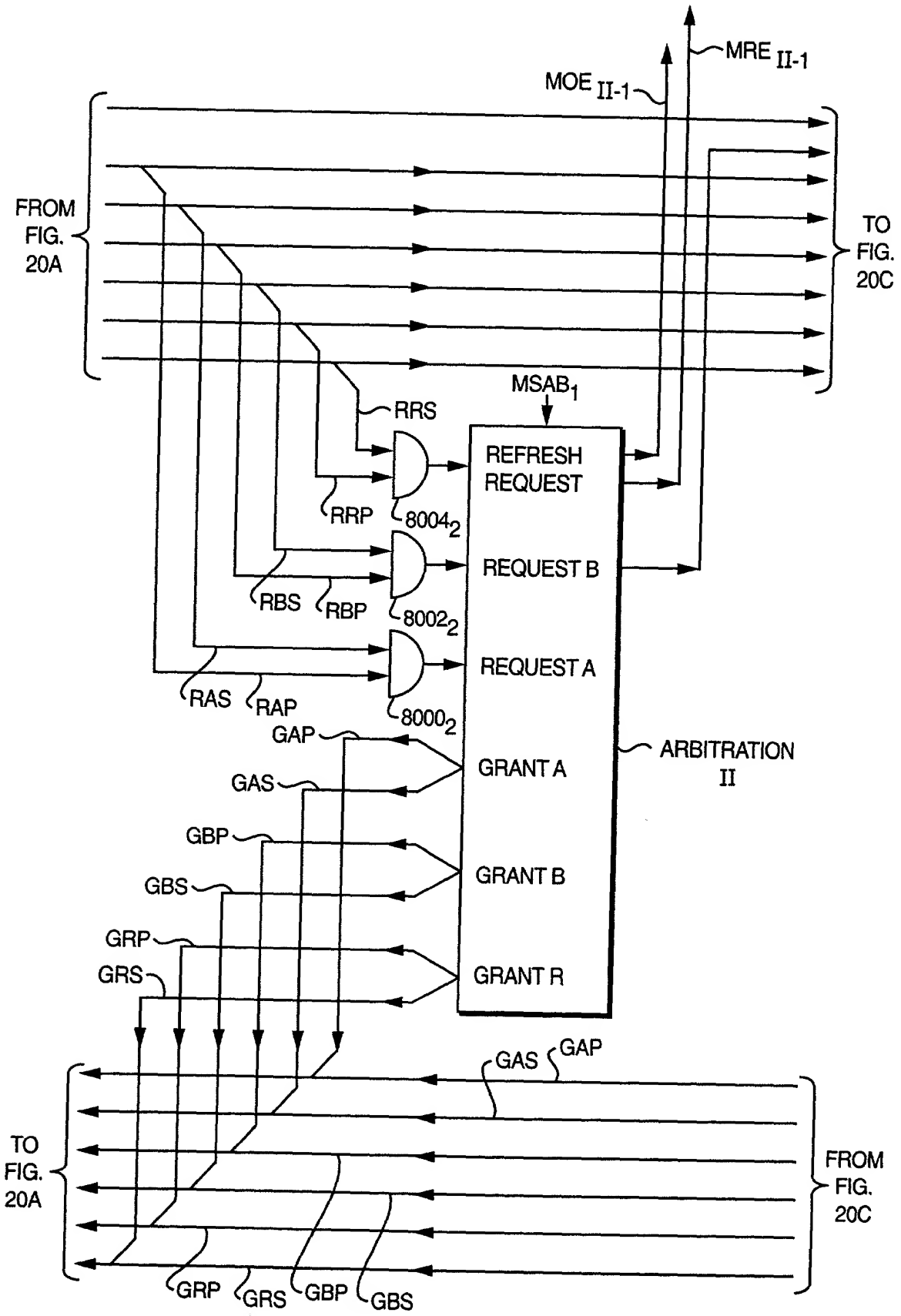

MRE II-1
MOE II-1
FROM FIG. 20A
TO FIG. 20C
MSAB1
RRS
RRP
8004 2
REFRESH REQUEST
REQUEST B
RBS
RBP
8002 2
REQUEST A
RAS
RAP
8000 2
GAP
GAS
GBP
GBS
GRP
GRS
GRANT A
GRANT B
GRANT R
ARBITRATION II
GAS
GAP
TO FIG. 20A
FROM FIG. 20C
GRP
GRS
GBP
GBS

FIG. 20B

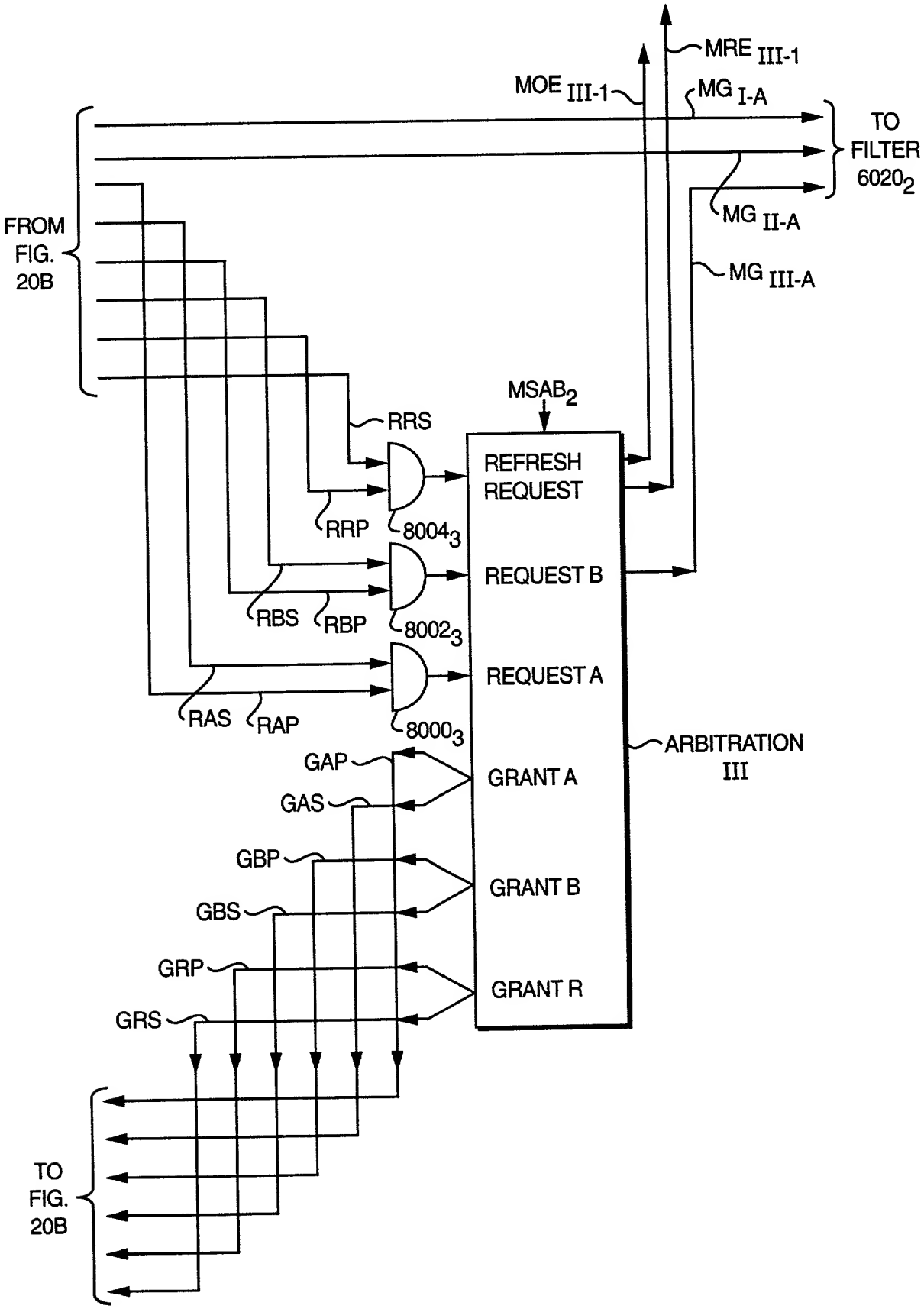

MRE III-1
MOE III-1
MG I-A
TO
FILTER
6020$_2$
MG II-A
MG III-A
FROM
FIG.
20B
MSAB$_2$
RRS
REFRESH
REQUEST
RRP
8004$_3$
REQUEST B
RBS
RBP
8002$_3$
REQUEST A
RAS
RAP
8000$_3$
ARBITRATION
III
GAP
GRANT A
GAS
GBP
GRANT B
GBS
GRP
GRANT R
GRS
TO
FIG.
20B

FIG. 20C